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SMUT - SERIAL MULTI-USER TERMINALS SYSTEM
MAINTENANCE MANUAL

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ABSTRACT

This manual describes the function and conventions used in the SMUT system, particularly the operation of the terminal control unit and the separate card function blocks.

FOREWORD

This manual has been written in the fond hope that it will provide solace to the harried maintenance person and perhaps make his or her task a little easier. The main trouble in understanding the operation of the terminal is the large number of tasks and variations on them than can be performed by the user and the subsequent allocation of faults to the IBM3031 or NOVA tasks and actual SMUT transmission faults.

Many faults occur because the user is presented with a large number of extra switches on a visual display unit or decwriter. Most of the faults that appear to be attributable to SMUT will turn out to have been caused by the user him(or her)-self in incorrectly setting one or more of these switches, particularly the baud-rate and line-local settings.

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(Continued)

1. INTRODUCTION

The SMUT [Ellis 1976] system has followed as a necessary expansion of the AAEC's computer link or Dataway. It was developed to rid the Dataway of inefficiencies caused by driving single-byte input-output devices such as teleprinters, page printers, and video display terminals.

SMUT has been implemented with the capability of operating many input-output devices using a single unlooped transmission line. The operations on this line are controlled on a polling basis by a minicomputer which is connected either directly or indirectly to the Dataway. This connection allows the minicomputer and consequently any of the SMUT stations to use the much larger facilities of the main IBM370 computer.

There are three SMUT systems in operation which use three independent co-axial cables laid in parallel for most of the route. These are referred to as Marks I, II, and III and they use cables I, II and III respectively. The systems are basically similar but differ in transmission levels and functional capabilities.

2. IMPLEMENTATION

2.1 General

Every SMUT system consists of a series of stations each comprising a terminal, usually a teleprinter operating at 110 baud or a decwriter operating at 300 baud, and a drive unit. These stations are connected to a single co-axial cable which extends approximately 1200 metres excluding stubs. The main cable run interconnects about 13 buildings at the AAEC's Research Establishment with 20 junction boxes (entry points) at convenient locations. The cable is terminated at the remotest points and stubs are unterminated. All entry points can be extended to connect multiple stations.

Each SMUT system contains a complex controller which polls the series of stations at a regular rate. Every station has a unique 7-bit address and will only respond to that address. The station communicates to the controller with a reply frame immediately it has been polled, the reply address being the station address with the controller bit asserted. All transmissions consist of three 8-bit bytes, an address byte, a status byte and a data byte. The address byte is composed of a write bit, a controller bit and an effective 6-bit address which permits 64 stations. The status byte includes reader and writer busy, channel end and device end with two spare bits. The data byte is generally an ASCII character with either a parity bit or mark bit, depending upon the input-output device.

The actual transmission used consists of a start bit, address byte, status byte, data byte, address byte complemented, and two stop bits. The address byte and the address complemented byte are compared by the receiver as a transmission safeguard. The transmission code is 35 bits long and is sent at 100 kbaud. Each station will transmit when a valid poll is received thus taking approximately 700 μs for a poll and reply. The controller operates at approximately 1 kHz which allows for some programming overlap.

2.2 Cable Junctions

The SMUT cable is nominally 70 ohm impedance. Three cables are laid, two for use (Marks I and II) and one for development (Mark III). The cables are tapped and joined at the entry points which are standard 50 ohm BNC connectors. No special care has been taken to keep impedances constant. Normally 50 ohm co-axial cable is used to connect the station to the entry point for short runs.

2.3 Cable Signals

The cable signal convention for Marks I and II is high (8 V to 12 V) for zero and low (0 to 4 V) for assertion, whereas Mark III operates low (0 to 2 V) for negation and high (4 to 10 V) for assertion. The actual level of a particular signal depends upon the distance between the observing and the transmitting points, because of the series resistance or attenuation of the cable. The SMUT cables are terminated at the remotest points with 2Zo (150 ohm) resistors to 12 V (Marks I and II), or to ground (Mark III).

2.4 Identification

All junction boxes are small diecast boxes (approximately 90 by 120 mm) mounted on a wall or other suitable position. Cable entry is normally via the short sides, and external sockets are normally face down on the lower long side. The main junction points have fuses mounted on the upper side which allow some protection against surges induced on the line. Socket I will be on the left when viewed from the lid with the external sockets down.

3. OPERATION

3.1 Function

The types of data transfer at the AAEC are quite typical and fall into three generalised areas:

1. Batch applications such as remote job entry and retrieval which are typified by relatively large quantities of input and output data per job. In these applications the control overheads should be kept as low as possible given that error detection and recovery are good enough to proceed without close attention by an operator.

2. Conversational computing where the traffic is balanced and operates on a character-by-character basis from an operator-controlled terminal. Most messages are short but the response times have to be minimal. The error detection and recovery can be controlled within reason by the terminal user.

3. Inquiry applications which consist of quite short input messages and relatively long output messages. The inquiry input has much the same constraints as for the conversational area. The output, however, can be quite large and should be as fast and error free as possible.

The batch application area is catered for by the faster, parallel Dataway link. The conversational area is serviced by SMUT. Here the input messages are at slow typing speeds. Errors when they occur can be deleted and retyped in most instances. The inquiry area is also serviced by SMUT.

3.2 Polling

Polling was used to overcome the possibility of overlapped transmissions. This increases the complexity of the controller but permits a much simpler design for the station. However, polling the stations results in slightly slower responses for the input-output terminals and increases the programming overhead for the controlling computer.

As a station will respond only to a unique address, the address byte on the reply frame is not needed. Using one bit of the address to specify station or controller return address enables the transmission frame to be kept constant, greatly simplifying receiver-transmitter design. The controller should accept a reply frame only if it receives the expected return address but the redundancy in the code practically guarantees that the reply address will be correct. This also makes it possible to separate the transmitter and receiver functions in the controller algorithms.

The controller transmitter-receiver pair can be tested by sending a poll with the controller bit set so that the controller will receive its own transmission which can then be cross-checked.

3.3 Terminal Speeds

The maximum speed at which the terminal can operate depends upon its baud rate. This speed can be achieved only if the next character is available as soon as the current character is complete. This requires instant attention from the controlling device whenever the printer becomes ready or whenever the keyboard receives a new character.

In a polled environment, a terminal will become ready but will have to idle until the next poll to the station is received. The maximum speed at which the terminal can operate is governed by how often the station is polled. When the poll is at a constant rate, as for a simple control program, then the minimum period per character is the smallest multiple of the poll period that is greater than the minimum period attainable by the terminal with immediate attention. For example:

> If the polling computer polls 27 terminals at 1 kHz then a teleprinter will operate at 9.2 characters per second on a print stream and the minimum period = 27 x 4, i.e. 108 ms per characters. (cf. normally 10 characters per second or 100 ms per character); and a decwriter will operate at 18.5 characters per second on a print stream and the minimum period = 27 x 2, i.e. 54 ms per character. (cf. normally 27 characters per second or 36.6 ms per character.)

This example gives an idea of how character rates depend on poll rates but character buffering and 'smart' polling will mask the effects of slow polling rates except in cases of chronic traffic congestion when the 'smart' poll algorithm breaks down.

3.4 Character Buffering

Because of the delay that occurs between a character being received and the station being polled, another character can start to be received before the current character has been read. When this occurs a non-buffered character can be partly cleared or garbled if the receiver accepts the incoming character; conversely the incoming character may be ignored or garbled. This problem can be accentuated by using the keyboard repeat feature. When a character is buffered as soon as it is received, fast access is not necessary and the polling rate can drop to about 2 polls per character before overrun occurs, instead of requiring immediate service. Buffering is accomplished by using an L1475 register which is bypassed when a Universal Asynchronous Receiver-Transmitter (UART) is used (see below).

A similar situation occurs when characters are to be printed at the maximum possible rate. When an output character is not buffered, the maximum rate will depend critically upon the poll speed. This is the case when one of the older units, which have an L1590 serial transmitter, is used. When the output character is buffered in the station, the terminal can operate at its maximum printing speed if enough polls are received to keep the secondary buffer full whenever the transmitting buffer has completed a character.

Development of the UART has made these buffering techniques currently available on chip. The more recent SMUT stations use these devices (L1580) which enable a marked increase in output speed but which do not decrease the polling delays on input. However, the input buffering allows more effective control of the keyboard especially when the teleprinter papertape reader is being used.

3.5 Smart Polling

Each SMUT controller is interfaced to a separate NOVA minicomputer with 24 k words of core memory. This enables the controller to operate a complex poll sequence without significantly reducing the memory available for user programs. Smart polling is designed to permit the use of video displays on the system because they require high poll rates to operate at reasonable speed and this reduces the number of polls available to service slower terminals. Smarter poll sequences were developed to increase specific poll rates without significantly reducing overall performance even at stations which have not been installed or are not in constant use. The basic problem was to define usage for operator convenience, and still keep display operation feasible. The specifications used in defining the smart poll algorithm are that

1. all stations capable of operating are polled;

2. all proposed stations up to a sensible maximum are polled at a slow rate to allow installation and maintenance without constant program modification;

3. only those stations that are currently being used need to be polled at the higher rate;

4. a station is considered to be used when it commences printing a line or message; and

5. a station is considered to be unused at some fixed time after the last line is started.

The algorithm is implemented by creating a primary address table which uses three out of four polls and which expands or contracts according to usage. The remaining one poll in four is used to scan sequentially the block of addresses from 63 to 0 regardless of speed of operation or expected usage. Entries are placed into the fast poll table whenever a line is started at a station and are deleted 10 to 12 seconds after the last character is sent.

The smart poll technique is still current and has proven very satisfactory because, as well as increasing printing speed for all fast poll stations, the conversational response is very good as long as input characters are echoed at better than the 10 s usage time-out.

When a terminal logs on and the fast table is full, the responses will be very slow until a fast table entry location is available. The slow responses will generally only occur at peak periods and in maintenance situations. One of these is when either the NOVA820 or NOVA1220 (Mk II) is down and all the SMUT terminals have been transferred to one computer thus causing an artificially high traffic situation. Another case is when the site computer has been down for an IPL or maintenance; upon restart, users who are tidying up jobs cause a peak in traffic for up to 60 minutes.

4. SMUT SEQUENCES

The two basic sequences used by SMUT are a write to a station and a read from a station. All other status responses are covered by these two fundamental sequences because they completely define the scope of a station. The write and read sequences have been made as symmetrical as possible so that a station could communicate with other stations if required but this usage has not been implemented in the current system. The sequences operate on a handshake basis wherever practicable so that a fixed response is expected for each operation. This has been used to try to overcome the effects of lost or garbled transmissions.

4.1 Controller Write Sequence

(See also Section 4.5)

When the controller writes to a particular station the sequence is commenced by the controller setting the Write address bit and setting the data byte to the required character on the next poll to the station. If the station is not busy, the write will be accepted, the station will reply CERO (Channel End Reader Out) on the return poll and proceed to print the character.

On the next poll to the station, the controller will set CEWO (Channel End Writer Out) to acknowledge the channel end received on the previous poll. When the station receives the channel end, the CERO bit is dropped on the return poll.

The write phase of the sequence is now complete. When the station reader becomes ready after printing the character, then DERO (Device End Reader Out) will be sent as a return to some subsequent poll. The controller will acknowledge the device end on the next poll by replying CEWO which will drop the station DERO.

The sequence above specifies the controller write completely but in actual operation a shorter sequence is used. The short sequence ignores the device end response and tries to write to the station on every poll. Whenever a CEWI (Channel End Writer In, i.e. CERO from the station) is received at the controller then the next character is sent on subsequent polls. The poll delays caused by waiting for a ready response are avoided and approximately half the polls per character are required. The station will respond busy status to all write requests when the printer is not ready.

4.2 Controller Read Sequence

(See also Section 4.5)

The read sequence is practically a mirror image of the write sequence except for the timing of the poll sequences. The sequence is initiated when the SMUT controller sets DERO when a character is expected or required by the operating system. When this bit is received at the station as DEWI (Device End Writer In) the papertape reader will be enabled (if present) and CEWO will be sent on the return poll. BWO (Busy Writer Out) will be sent on all return polls while the papertape reader is enabled, i.e. until a character is received.

When the keyboard receiver has received a character, from either a papertape reader or a keyboard, the station will idle until the next poll from the controller. The station will set the write address bit, DEWO (Device End Writer Out), and set the data byte to the received character on the return poll.

If the controller will accept the character then CERO will be sent on the next poll to the station. When this bit is received, DEWO is dropped and the write request is cleared. This is indicated by CEWO being sent on the return poll.

4.3 Address Bit Assignments

Bit 07 - Set whenever the character in the data byte is to be written. This bit will generally coincide with the Device End Reader In bit (DERI).

Bit 06 - Set whenever the transmission is a return from the station. It may be set by the controller for diagnostic purposes to check a transmitter-receiver pair.

Bits 05-01 - Address bits used for polling the stations (0 to 63).

4.4 Status Bit Assignments

Bit 07 - Attention Writer In, Reader Out. This bit is currently not used and is unlikely to be used for this purpose. It is set to zero.

Bit 06 - Busy Writer In, Reader Out. This bit is an indicator that the writer (keyboard) is receiving a character. Busy signal from the printer transmitter.

Bit 05 - Channel End Writer In, Reader Out. When received by a station this bit clears DEWO (Device End Writer Out) and sets CEWO (Channel End Writer Out). When this bit CERO is sent it signals that the reader (printer) accepted the last character.

Bit 04 - Device End Writer In, Reader Out. When this bit is received by the station then the next character is requested, i.e. the advance solenoid is actuated for a teleprinter papertape reader. When sent, DERO signals that the reader (printer) is ready for another character.

Bit 03 - Attention Reader In, Writer Out. This bit is not used

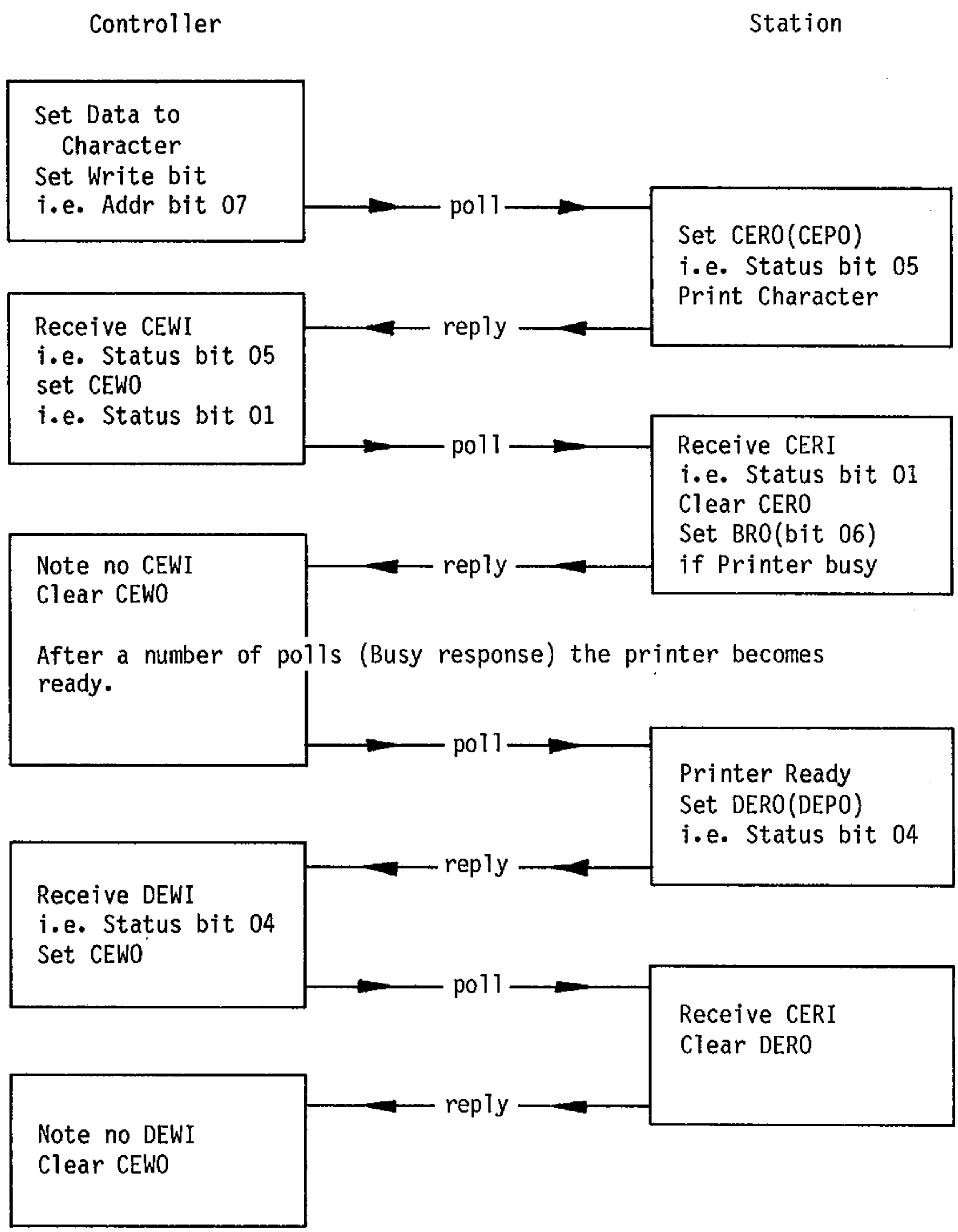
Bit 02 - Busy Ready In, Writer Out. This bit is an indicator that the reader (printer) is printing the last character. Busy signal from the writer (keyboard receiver) which covers the period that the papertape reader would have been actuated.

Bit 01 - Channel End Reader In, Writer Out. When received by the station this bit clears Device End Reader (printer ready) and acknowledges that channel end was received by the controller. When sent by the station CEWO indicates that CEWI or DEWI was received from the controller.

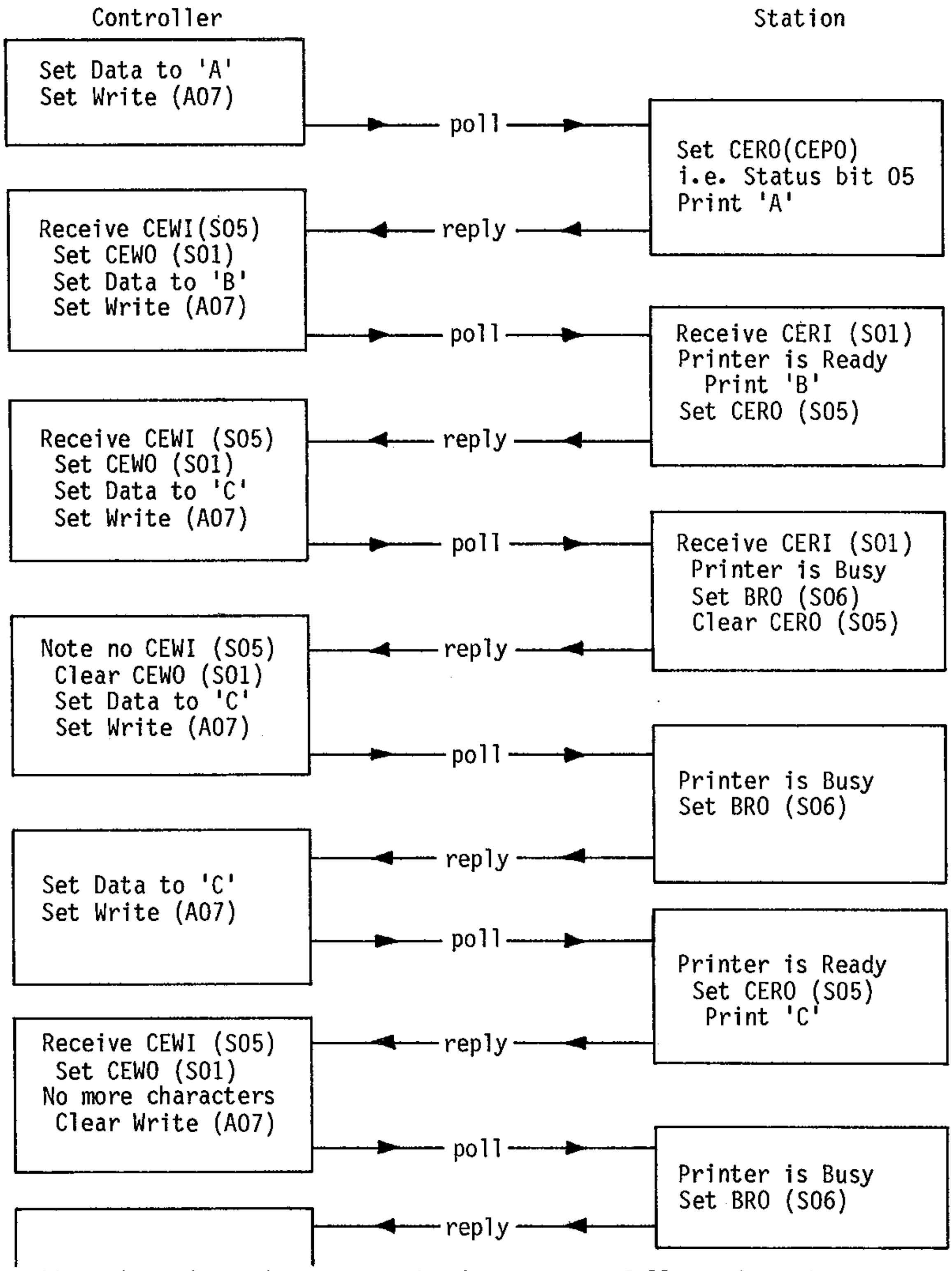
Bit 00 - Device End Reader In, Writer Out. Indicates another character is ready for the reader (printer). DEWO indicates that a character has been received and is present in the data byte.

4.5 Sequence Flow Diagrams

The controller Write sequence is outlined below, showing polls to one station only.

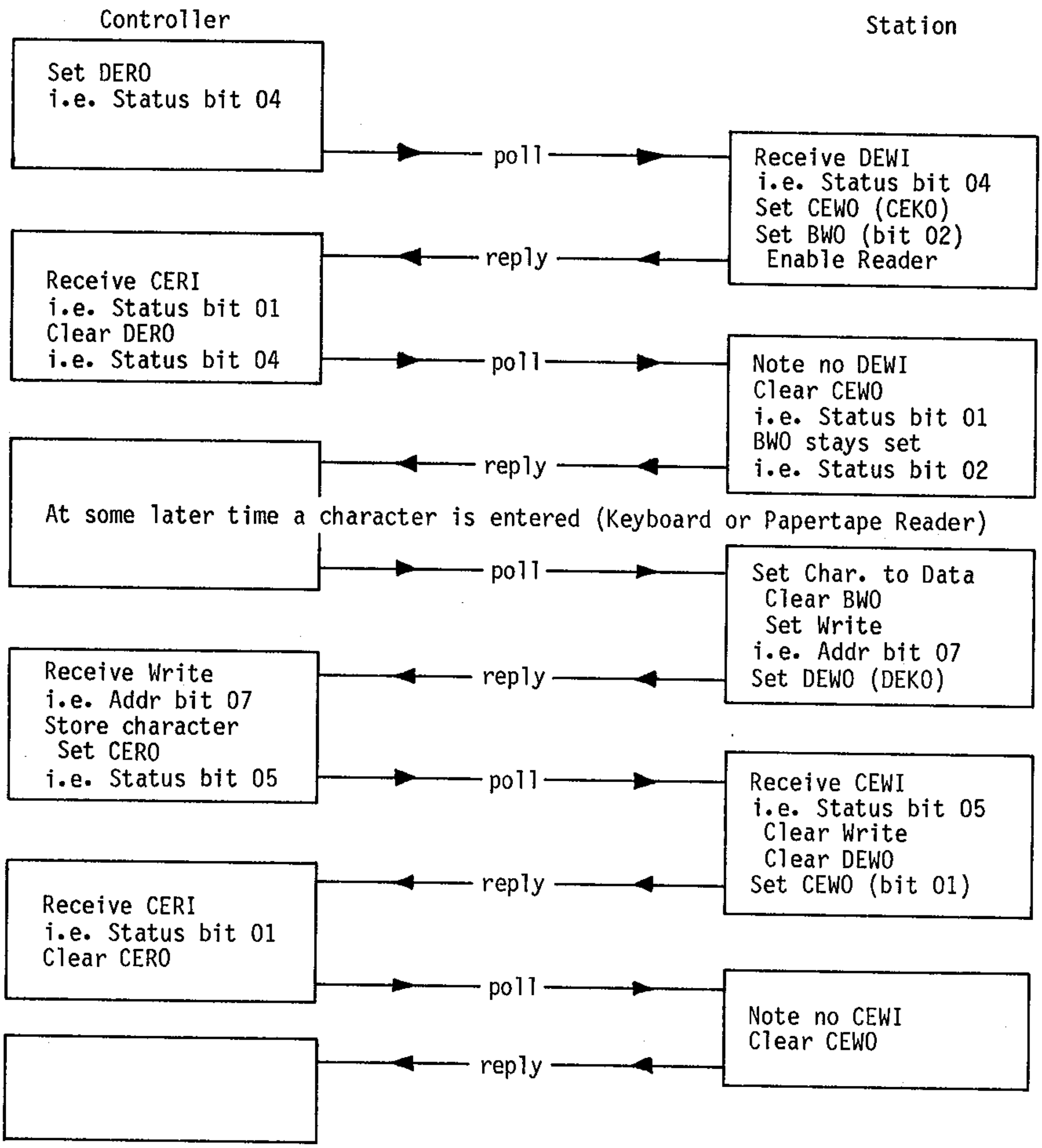


The controller Short Write sequence is outlined below, showing polls to one station only and printing the string ABC.



When the printer becomes ready the sequence follows the Write sequence.

The Controller Read sequence is outlined below, showing polls to one station only.



For clarity several status bits have been labelled according to their terminal function (i.e. P for Printer, K for Keyboard/Papertape Reader).

4.6 Frame Bit Positions

Two sample transmissions are listed to show bit positions within the frame and function of each bit. The status bit functions at the controller and station are complementary and are specified separately. The addr and addc bits are logical complements within each frame. The address used is 1C hexadecimal and the character used is A (C1 hexadecimal).

	Write from Control to Station				Status from Station to Control			
Bit	Control	Function	Station	Function	Station	Function	Control	Function
01	start	= one	start	= one	start	= one	start	= one
02	addr 07	= one	addr 07	= one	addr 07	= zero	addr 07	= zero
03	addr 06	= zero	addr 06	= zero	addr 06	= one	addr 06	= one
04	addr 05	= zero						
05	addr 04	= one						
06	addr 03	= one	see column 1		see column 1		see column 1	
07	addr 02	= one						
08	addr 01	= zero						
09	addr 00	= zero						
10	stat 07	= zero	stat 07	= zero	stat 07	= zero	stat 07	= zero
11	stat 06	= BRO	stat 06	= BWI	stat 06	= BRO	stat 06	= BWI
12	stat 05	= CERO	stat 05	= CEWI	stat 05	= CERO	stat 05	= CEWI
13	stat 04	= DERO	stat 04	= DEWI	stat 04	= DERO	stat 04	= DEWI
14	stat 03	= zero	stat 03	= zero	stat 03	= zero	stat 03	= zero
15	stat 02	= BWO	stat 02	= BRI	stat 02	= BWO	stat 02	= BRI
16	stat 01	= CEWO	stat 01	= CERI	stat 01	= CEWO	stat 01	= CERI
17	stat 00	= DEWO	stat 00	= DERI	stat 00	= DEWO	stat 00	= DERI
18	data 07	= one			data 07	= any		
19	data 06	= one			data 06	= any		
20	data 05	= zero			data 05	= any		
21	data 04	= zero	see column 1		data 04	= any	see column 3	
22	data 03	= zero			data 03	= any		
23	data 02	= zero			data 02	= any		
24	data 01	= zero			data 01	= any		
25	data 00	= one			data 00	= any		
26	addc 07	= zero	addc 07	= zero	addc 07	= one	addc 07	= one
27	addc 06	= one	addc 06	= one	addc 06	= zero	addc 06	= zero
28	addc 05	= one						
29	addc 04	= zero						
30	addc 03	= zero						
31	addc 02	= zero	see column 1		see column 1		see column 1	
32	addc 01	= one						
33	addc 00	= one						
34	stop	= zero	stop	= zero	stop	= zero	stop	= zero
35	stop	= zero	stop	= zero	stop	= zero	stop	= zero

5. OPERATING EXPERIENCE

As the number of terminals has increased, faults caused by cable length, reflections, etc. have become more apparent. These faults are more noticeable during high traffic periods.

5.1 Effects of Dropouts

The transmission code consists of four basic bytes - the address byte, the status byte, data byte, and the address byte complement. The address bytes are compared when the transmission is received and if the first byte does not match the complement of the last then the complete transmission is rejected. This format was adopted because if the leading and trailing bytes could be guaranteed then the central bytes should be more reliable.

The likely ways that incorrect performance can occur are either by the loss of the outward or return poll or by the incorrect reception of individual status or data bits. Although much effort has been made to ensure correct transmission, dropouts will occur. When a data bit is dropped, the echo will be incorrect. This can be deleted and retyped by the operator. When a status bit is dropped, the system, which operates in a in a semi-handshake mode, can usually cope. In a few known instances the system may fail, particularly when the dropped bit was a Channel End.

5.2 Loss of Channel End on a Write

When either the controller or the station sends a character, using the short sequence (4.1), the correct Channel End response is vital as the sender will keep sending the character until this Channel End is received. If, for example, the controller write sequence is used, the station will accept the write and then reply Channel End on the return poll. If this return poll is rejected because of mismatch, or if the CEWI bit is lost, then the controller will keep sending the character. On the next outward poll when the station receives the next write the Channel End bit will not be sent as the terminal is busy and the station will not accept the character. As the controller will keep sending the character, double printing will result. A classic example of this fault occurs when the station transmitter has failed and no return polls are received. In this case, the first character to be sent to the station will be printed indefinitely. A different method would have been to keep the Channel End active until it is cancelled but as this can cause lost characters it was considered the greater evil. A similar result occurs when the Channel End is lost on the outward poll during the read sequence from the controller. In this case, the double print will be two valid input characters, both of which have been accepted.

5.3 Loss of Device End

When the system is relying on the successful receipt of a Device End, a stall may result. If the Device End is dropped, for example, in the operation of a terminal papertape reader, and cancelled by a valid Channel End, the station will not start the papertape reader. This particular fault has been minimised by changing the keyboard busy signal to cover the period between energising the solenoid and receiving the next character. When the controller expects a character from a station that is flagged as not busy, another Device End is sent. The converse problem occurs when the controller relies upon the Device End before writing the printer character. As this is not a problem with the short write sequence it has been ignored.

5.4 System Lockup

Because the SMUT controller is program controlled it can have program delays when the computer is handling interrupt requests from direct connection teleprinters, Dataway transfers, etc. Such requests can delay the outward poll when the clock interrupt is taken late. When delays exceed 300 μs, there is a possibility that an undelayed outward poll will be sent over a delayed return from the previous outward poll. The computer tests receiver busy before issuing an outward poll so if the receiver is busy with the return poll then the overpoll is delayed one clock interrupt.

This test enabled a fault to be found in the receiver logic design. There are two common methods of detecting the end of an incoming transmission; either to start a counter and count off the incoming bits until the counter is zero, or to shift the start bit through a shift register of the right length until it falls out. The L3570 receiver uses the second technique, and very occasionally noise pickup and variation in gate switching thresholds cause the receiver to be set busy without the start bit being set in the shift register. When this occurs, the receiver remains busy until the next poll when another bit is detected and shifted through. The failure to clear busy until the next poll is incidental unless the receiver that is incorrectly set into the busy state is the controller receiver which, because of the possibility of overpoll, as mentioned above, will stop the next poll and prevent any chance of clearing the busy state.

This lockup state can be cleared by earthing the cable to assert the signal (Marks I and II) or by waiting for the computer to clear the fault when the inactivity is detected (see below). When an updated SMUT receiver (L3572 linked for L3570 operation) is used in the controller interface, this lockup state does not occur.

Lockup states have occurred when a mask or enable flip-flop has been set or cleared by a transient signal. The DATERCOM system has a time-out loop which is entered when SMUT activity ceases for any reason. If this loop times out, the computer re-initialises the controller interface flags and interrupt masks, generally within 20 seconds, and the transient state is cleared.

6. FUNCTION BLOCKS

This section describes the operation of the particular printed circuit cards used by the SMUT stations. The actual cards may be modified from time to time to improve performance should the need arise. These modifications will be updated on the appropriate engineering drawings which should be used for maintenance. The function of each card will remain the same as the system is stable and development is no longer in progress.

6.1 SMUT Transmitter (L3590)

The SMUT transmitter takes 24 bits of information in parallel and sends it as a SMUT frame, i.e. a start bit, address byte, status byte, data byte, address byte complemented and two stop bits. The data are loaded within 200 ns of the positive edge of TXL (Transmitter Load), the eight address input bits are negative assertion, the status and data bits being positive assertion. The L3590 adds the start bit, address complement byte and stop bits, and transmits the serial stream at ten times the input clock period. For SMUT this input (TTC) is 1 MHz.

The L3590 drives to ground for assertion and drives to high for negation (10 V). Although the positive drive is transient it is not active unless the transmitter is sending.

There is a series of L3590 cards that are wired on L3592 printed circuit cards. These cards are functionally identical except that they are changeable by linking to drive high for assertion. The L3590 ex-L3592 will drive only if the transmitter is busy (TXB) and the output is tri-stated when not busy. This model L3590 is the current production model and will occur more often in units with higher serial numbers.

6.2 SMUT Receiver (L3570)

This SMUT receiver accepts a SMUT frame in serial and, after transmission checks are performed, presents the data in parallel format. The receiver input is filtered and shaped, and monitored continuously for an asserted edge. If the signal is still true after four clock periods, the receiver shift register is cleared, and the input stream is shifted along the shift register every ten clock periods until the start bit reaches the final stage. When this occurs the address and its complement are compared and the stop bits are checked for zeroes. If the address match and the stop bits are correct then the AOK (Address OK) signal is asserted.

The receiver has a match enable input which when negated disables the match circuitry to enable easier debugging of the unit under maintenance conditions.

Inputs to the L3570 are the clock (TRC), line in (LINE) and TEST signals. LINE is ground assertion and 10 V negation. TRC is a pulse train at 10 times the baud rate (10 x 100 k = 1 MHz) and TEST is a negative TTL level for match disable.

Outputs from the card are Line Out (LO), Transmission Receiver Busy (TRB), Address OK (AOK), Address Out Conditional (AOC), and the 24 data lines. AOK signifies that a frame has been received correctly, AOC signifies that a frame has been received and LO shows the state of the input line after the filtering and shaping stage. TRB indicates that a transmission frame is being received.

The alternative type of receiver is an L3570 loaded on an L3572 printed circuit board and linked for L3570 operation. The function of the card is identical to the original but the receiving method is different. In this case, when start is detected a counter is cleared, the shifts are counted in a scaler and a pulse is generated on overflow, indicating that the complete stream has been received. The match circuitry operates in the same way but uses more modern chips.

6.3 SMUT Address, Status (L3580)

This card performs the basic control and response functions of the SMUT station. These are

(a) Comparison of the Address Out (A00-A06) bits received with the Address Selected (AS0-AS6) bits. The AS0-AS6 bits are link selected and are the complement of the required station address. AS0-AS6 are also used as the transmission address for the L3590 and are negative assertion (see above). The address bits are compared, using exclusive or gates for each bit, and the outputs anded with AOK generated from the L3570 output. The resultant strobe (CTS) which signifies that correct transmission and correct station have both been satisfied, is used to synchronise all control operations.

(b) Synchronisation and latching of the two levels that could vary during CTS, the keyboard ready and the printer busy (KRR and TWB). Both of these signals are used as return frame status bits as well as specifying control operations.

The following functions are then performed:

(c) If A07 is set (i.e. write) and the latched busy status (RBS) is zero (i.e. not busy) then a TLS (see below) is issued to print the character in the received data byte, and CERO is set. If RBS is set, no TLS is issued and CERO is not altered.

(d) If the latched KRR is set, AS7 complement will be negated so that a write will be sent on the return frame.

(e) If DEWI is received, KFC (see below) is issued and CEWO is set.

(f) If CEWI is received, KCR (see below) is issued and CEWO is cleared.

(g) If CERI is received, TCR (see below) is issued and CERO is set.

(h) When all the above conditions have stabilised, TXL (Transmitter Load) is issued and the return frame is sent. TXL is simply a delayed version of CTS.

6.4 Teletype Transmitter (L1590)

A teletype or similar terminal requires an 11-bit code (sometimes 10 for faster devices); a start bit, eight data bits, and two stop bits (1 for faster devices). The L1590 can be loaded with an 8-bit byte or character in parallel whereupon the byte will be sent to the output device in serial, with the start and two stop bits added. The output device is driven to ground in the idle state and either a 20 or 60 mA current loop can be set up by means of an appropriate resistor from a positive supply using the TeleType Output signal (TTO).

The clocking of the serial out data is generated from the input clock (TTC) using a SN7490 decade counter; thus the clock input required is ten times the required baud rate. There is no restriction on speed for the usual range of 110 to 9600 baud.

Inputs to the card are the Teleprinter Load Sequence (TLS), TTC and Teleprinter Clear Ready (TCR) as well as the eight input bits. Both TLS and TTC are negative-going edges whereas TCR is a positive-going edge. The outputs are TTO, Teletype Writer Ready (TWR) and Teletype Writer Busy (TWB), both TWR and TWB being positive assertion.

6.5 Teletype Receiver (L1570)

The teletype receiver accepts a data train similar to that produced by the transmitter (see above). Receipt of a character is accomplished by shifting the input stream through a shift register until the start bit is set into the last position of the register. When this has occurred the stop bits are checked and, if zero, the Keyboard Receiver Ready (KRR) flip-flop is set. The input stream is monitored to guard against a noise signal which will cause a spurious character and the serial code is shifted at approximately the centre of each bit. The clock signal TTC is set to 10 times the required baud rate and any input must be present for at least four clock periods before it is accepted. The input current loop is about 20 mA from TTI (TeleType Input) to ground, the active pull-up coming from the L1570.

The input of this card is R-C filtered when received and this filter time constant must be modified if faster devices are used. Normally 100 ohm and 4.7 μF are used for a teleprinter (110 baud) and decwriter (300 baud) and a smaller capacitor is used for higher speed devices. The capacitor is removed entirely for 2400 baud and above because the incoming signal is quite clean and has no contact bounce with the existing video-display terminals.

Inputs to the card are TTI (above), TTC, Keyboard Clear Ready (KCR) and Keyboard Reader Enable (KRE). KCR, which is used to clear the Keyboard Reader Ready (KRR) flag after the input character has been processed, operates on a positive edge. KRE is used to actuate the Keyboard Reader Solenoid (KRS) output which drives to ground when a character is required. The KRS output can drive about 100 mA from a positive pull-up. The Keyboard Reader Busy (KRB) indicates that a character is being received, i.e. the start bit has been verified. KRS will switch off when KRB goes positive.

6.6 Combined Transmitter Receiver (L1580)

This card performs the function of both teleprinter transmitter and receiver and uses an on-chip UART. The more recent SMUT stations have been wired so that appropriate connections of the L1570 are wrapped onto the L1590 position (A1), enabling either an L1570-L1590 pair or an L1580 to be used as alternates. The signal functions are equivalent except that the L1580 has an inbuilt baud rate clock which is independent of TTC and does not depend on the clock card jumpers. The clock frequency is set to 16 times the required baud rate, the coarse adjustment by changing capacitor C1* and the fine adjustment by altering the trimpot position (RV1). Slightly better reliability will be obtained by setting the period about 1 per cent high. When high baud rates are used, the input filter capacitor (C2) must be lowered and can be removed if the keyboard input signal is not noisy.

There are two types of UART used, both pin compatible but one requiring a negative (-12 V) supply rail. This type (MM5303, COM2502) uses an on-card negative supply derived by voltage doubling the output of an LM555CN timer which is used to chop the 10 V supply rail. On cards where a TR1863 UART is used, the -12 V components need not be loaded. When an L1580 is used the UART has its own character buffering and the L1475 (below) can be bypassed using a jumper card. The operation will not be affected if the L1475 is left in.

* Note. This must be a stable type)

6.7 Clock (L1065)

The clock card is capable of selecting two independent clock trains both derived from a 10 MHz crystal oscillator and using two decade divider chains.

Both trains use a 1 μs clock as the basic unit, one chain capable of selecting 1,2,10,20,100,200 and 1000 μs as the clock period whereas the other selects any period from 1 to 400 μs in 1 μs steps or any period from 400 to 998 μs in 2 μs steps. The different periods are link selectable using soldered links on the L1065 card. The first clock is used for the 1 μs SMUT input clock to the L3570 and L3590, whereas the more flexible divider is used to generate the ten-times baud rate clock for the L1570 and L1590. Both negative and positive pulse trains are generated for each divider chain, the output being about 300-500 ns wide.

6.8 Buffer (L1475)

This card contains 12 latch flip-flops which are strobed in pairs. The latches are SN7475 and will transfer input to output whenever the strobe is high and will latch whenever the strobe goes low. If the strobe is left high, the latch can be used as a pulse shaper or level restorer. Eight latches are used for the keyboard buffer and one latch is used to shape the differentiated KRR strobe pulse. The card is used as a character buffer when an L1570 is used as the input device.

7. SMUT CONTROL UNIT

This section covers the hardware used in construction of the SMUT units which is incidental to the logical function.

7.1 Power Supply

The power supply, which supplies the +5 volt rail and the +10 volt unregulated rail, is derived from 240 volt 50 Hz which uses a standard Cannon connector. Lower serial-numbered boxes were supplied with an AAEC built unit, whereas current units are supplied with a commercial supply. The two units have similar specifications, the commercial unit having a slightly higher 10 volt rail (approximately 11 to 13 V) depending on load. Both supplies are capable of supplying 5 V at greater than 1.5 A which is about the upper limit for a SMUT unit. The supplies normally run quite warm and units should not have their airflow restricted.

The AAEC unit is built according to drawing A3E45877 which refers to the circuit diagram A3E46184. The commercial unit is a Statronics 53/5 with an extra lead to the unregulated supply. Both supplies use 500 mA delay fuses mounted directly beside the mains input plug/socket.

7.2 Surge Suppression

Line surges are limited with a fuse connected in series with the line in more recent SMUT boxes. The signal swing is limited to just below ground and to approximately 13 volts. The positive limit is derived from the unregulated 10 volt and uses a 12 volt, 5 watt zener to absorb spikes. If a large surge comes down the line, the series fuse will blow generally before damage is done. The fuse should be 250 mA and not delay or slo-blo. The fuse holder is mounted beside the SMUT line co-axial connectors. The surge suppression network, if fitted, is mounted on a printed circuit card which solders onto the line input connectors and contains all the extra resistors etc. for the terminal drive and also the isolation network (see below).

7.3 Line Isolation

Most SMUT units have a relay operated from the unregulated rail so that the unit is electrically isolated from the line when the unit is powered down. The relay contacts are in series with the line and the surge suppression fuse. This isolation saves loading the line with the receiver and back-biased driver circuitry when the unit is off and also provides an excellent chance of the unit surviving a lightning storm if it is switched off before (and not after!) any strike.

8. SMUT LINE CABLE

The SMUT cable has been modified considerably since it was laid. The many extra stubs laid from the main line to various rooms and laboratories around site have increased the chances of surges being picked up as well as degrading the signals on the line because of extra loading, reflections, etc.

8.1 Line Surge Suppression

The actual SMUT line has surge suppression networks mounted in several of the main junction boxes, generally the 52 mm deep variety. These have fuses connected between the line and the external sockets so that if a large surge is induced on the line then the subsidiary cables and units connected to them will be protected. The fuses in these boxes are mounted on the upper side or on the side opposite the external line connectors. Line 1 will have its fuse directly opposite its connector. The fuse should be 250 mA or 500 mA in higher noise areas and must not be a delay or slo-blo type.

8.2 SMUT Line Termination

There are two types of line terminators in use on the actual line; the main terminators are powered up, whereas the other type derive the positive rail from the line. These terminators are functionally a 180 ohm, or similar, resistor which is pulled up to 10 volts. The unpowered version uses a diode to charge up a capacitor when the line is high which acts as the positive rail when the line is driven. The powered version generates the positive rail from 240 volt 50 Hz unless the power is disconnected, whereupon the rail is derived from the line as for the unpowered models. There are powered terminators in the line repeater units (see below).

8.3 SMUT Line Repeater

Because of signal degradation on the longest run (approximately 1 km to Building 58) which had a permanent stub of approximately 300 m, a repeater had to be installed to enable reliable operation for several stations. Since then the stub (Buildings 55 and 21) has been removed but the repeater is still installed. The reliability of stations situated about halfway along the cable is enhanced by the repeater as this is where reflections would be expected to be greatest.

The repeater is bi-directional and consists of two receivers, two transmitters and direction control logic. Each input receiver is delayed and the direction is determined during this period. If the signal propagating down the line from the controller occurs first then the direction will be down and only the down driver will be enabled. If the direction is up then only the up driver will be enabled. The unit is not quite symmetrical because if the down line (i.e. beyond the repeater) is asserted for more than 1 ms then the direction will be changed to down and the up driver will be disabled. This procedure prevents a fault beyond the repeater from stopping the whole system.

The repeater is relay-isolated from the line and the line is reconnected when the unit is powered down.

9. NOVA INTERFACE

The controlling computer is required to service all terminals on the SMUT network, i.e. accept all input characters and send any replies or echoes. Currently the computer operates according to the Smart Poll algorithm (see 3.5) and also performs some basic error checks and corrections.

The computer requires two separate devices to control the SMUT network - the actual interface between the computer bus and the SMUT line, and a real-time clock which is used to control the transmission period and also to provide time-outs, etc. for system operation.

9.1 Real-Time Clock (RTC)

The real-time clock is driven from a 1 kHz frequency source derived from a 10 MHz crystal oscillator (see L1065). The RTC is decoded as device 14 octal and its interrupt is controlled by users of data bit 13 when the mask instruction is executed. The RTC instructions perform the functions

NIOS	14	Enable Clock, Clear Done Flag
NIOC	14	Disable Clock, Clear Done Flag
SKDN	14	Skips if Done Flag has been set by the RTC
SKB	14	Skips if the Interrupt Mask is enabled.

9.2 SMUT Control

This device is effectively two separate entities, the transmitter and receiver sections. The transmitter section consists of a 24-bit buffer register which is loaded with the address byte, status byte and data byte on independent commands. The buffer register is connected to the SMUT transmitter inputs (N.B. the address byte is inverted). These are transmitted on a NIOP or DOXP. The operating instructions are

DOA 15 Load Address Byte into buffer
DOB 15 Load Status Byte into buffer
DOC 15 Load Data Byte into buffer
NIOP 15 Transmit using data in buffer

The receiver section consists of the SMUT receiver, a buffer register used for storing the receiver contents at the last detected interrupt, the read logic, and the interrupt selection and assertion logic. The interrupt is masked by using bit 11 at mask out time. The receiver Done flag is set if significant status bits are present to minimise interrupt processing time according to the function

Set Done = A06.(A07+CEWI+CERI+DERI+BRI).AOK

where AOK is the correct transmission received signal and the other levels are standard (see Section 4). The reader buffer is loaded on the leading edge of the Done signal to prevent data loss if the interrupt is serviced too slowly. The device instructions are

NIOS 15 Enable Receive, Clear Done Flag
NIOC 15 Disable Receiver, Clear Done Flag
DIA 15 Read Address Byte
DIB 15 Read Status Byte
DIC 15 Read Data Byte
SKDN 15 Skips if Done Flag has been set
SKB 15 Skips if the Receiver is Busy (receiving a transmission)

10. ACKNOWLEDGEMENTS

The SMUT software interface with DATERCOM [Sanger 1976] was written by P.L. Sanger together with numerous refinements and diagnostic aids to improve overall system performance.

The SMUT hardware was developed with the help of J.D. Milne and P. Parton of the Digital Systems Group.

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12. GLOSSARY

baud	-	bit per second defining information transfer rate
byte	-	eight bits
controller	-	the computer and its interface to the SMUT network, i.e. the network controlling station
frame	-	the transmission block of start, address, status, data and stop
poll	-	a transmitted frame from the controller to a station which governs the station's right to send
reply frame	-	the response by the station to a poll
station	-	the terminal and its drive unit, particularly the drive unit
terminal	-	the input-output device that interfaces to the user, normally a teleprinter, decwriter or video-display

APPENDIX A
DRAWING NUMBERS

The engineering drawings for the SMUT system are myriad. The following subset should be all that is required for maintenance.

A2E45874	SMUT teletype station
A3E46184	SMUT power supply
CE40183	NOVA-SMUT input/output and card allocation
CE40184	NOVA-SMUT receiver control
CE40185	NOVA-SMUT clock interrupt
CE40186	NOVA-SMUT data paths
A2E43464	SMUT Repeater - mother board
A2E43465	SMUT Repeater - DSG020
A2E48076	L1580 - Circuit Diagram (CD)
A2E48077	L1580 - Component Layout (CL)
A2E48582	L3572 - CD
A2E48583	L3572 - CL
A2E48586	L3592 - CD
A2E48587	L3592 - CL
CE40674	L1065 - CD
CE40676	L1065 - CL
CE40662	L1475 - CD
CE40665	L1475 - CL
CE40628	L3580 - CD
CE40631	L3580 - CL
CE40439	L1570 - CD
CE40441	L1570 - CL
CE40443	L1590 - CD
CE40446	L1590 - CL
CE40165	L3570 - CD
CE40659	L3570 - CL
CE40457	L3590 - CD
CE40460	L3590 - CL

APPENDIX B
$ NOVA

The interactive program $NOVA [Backstrom 1979] is used to display diagnostic information supplied by the DATERCOM system [Sanger 1976].

The three types of displayed information presented by the program are

(a) A hexadecimal printout of 144 NOVA words (16 bits) of diagnostic information, consisting of 16 UCBs for Network Communication, and details of all active Terminal Control Blocks.

(b) A hexadecimal printout of 64 words of SMUT diagnostic information relating to lost and garbled polls, and 20 SMUT fast table entries.

(c) Details of terminals currently logged onto the DATERCOM system with some details of the particular tasks.

A colon (:) is issued as a prompt character by the NOVA programs, the responses being

1. Period (.) or Dataway address which gives details of users logged onto the system as in (c) above,

2. Single quote (') followed by period or Dataway address which gives the hexadecimal printouts (a) and (b) above followed by terminal details as for (c) above.

3. Hash (#) followed by period or Dataway address which gives the 64-word hexadecimal printout and 20 fast table entries (b) followed by terminal details (c).

4. Immediate carriage return which terminates the program which gives END:NOVA at the terminal.

Output to responses 2 and 3 is preceded by the number of bytes received, together with the time and date, and is followed by the number of bytes used by DATERCOM for control blocks and ACL-NOVA work areas.

The pertinent data for SMUT diagnostics are the 64-word SMUT diagnostic table, (a) the SMUT fast table (b) and the terminal occupancy list (c). The 20-word SMUT fast service table has the address+1 of the particular SMUT station in the high order byte and a time-out index in the low order byte. The SMUT diagnostic table gives details of lost transmissions and mismatches in two word elements, an identifier followed by an error count word. In the case of lost transmissions (polls) the high order byte of the first word of a pair will be 80 and the low order byte will be the SMUT station address followed by the error count word. For the mismatch pair, the high order byte of the first word will be the polled address with the received address in the low byte followed by the error count word. The SMUT diagnostic table can be cleared from the terminal (see $NOVA [Backstrom 1979]).

Note that $NOVA is a 3031 task and will not operate with the Dataway or main computer access unavailable.

APPENDIX C
LOCATION

The SMUT cable has been laid to approximately 25 buildings (including stubs) with about 50 entry points as well as the computer building (B51) which has 15 entry points. The total number of stations installed on both systems is approximately 50.

Currently serviced are buildings 1, 25, 16, 16E, 67, 64, 51, 3, 2, 56, 19, 14, 4, 22, 55, 53, 21A, 21B, 23A, 23B, 58 and 38.

A list of stations, with their location (building), responsible officer and phone number is kept on the IBM3031 and can be obtained from the author (PJE). This list also includes the serial number of the unit, its SMUT address, the actual input-output terminal and its operating baud rate. The list is kept reasonably up-to-date as it is also required by the 3031 as a basis for page-size for each individual terminal.

There are two SMUT systems and the stations are divided between them according to whim, usage, repeater location, and whether operation is more reliable. At present there are no two addresses that are alike so that units can be changed at random onto either system without address duplication overlaps. Because of this flexibility there is no list of which stations are connected to the Mk I or Mk II systems. Another major factor, in allocating which stations are controlled by which NOVA, is program development and this tends to constrain one system (Mk II) mainly to the computer building.