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COOLED PREAMPLIFIERS WITH N- OR P-SILICON JFET'S

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ABSTRACT

A voltage sensitive cooled preamplifier has been operated with comparable resolution from n-and p-Si junction field effect transistors (JFET'S). To obtain optimum JFET operating conditions it is necessary to consider in detail the inter-related parameters of device thermal resistance, the variation of JFET noise with temperature and of gate current with drain voltage. Measurement and optimisation procedures are described.

This work has been submitted to a journal. Further details can be obtained from the author or the Director of the Research Establishment.

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Figure 1 Equivalent input noise voltage versus drain volts for two 2N4416's from different manufacturers. The values marked are estimated device temperatures (r_t = 280°K/W). Curves A and B, device 4, T_C = 72°K; A, V_{GS} = - 1 V; B, V_{GS} = 0 V. Curve C, device 1, T_C = 84°K, V_{GS} = 0 V.

Figure 2 Equivalent input noise voltage versus drain volts for p-Si (Curve P) and n-Si (Curve N) JFET's. Curve N, 2N4416, T_C = 93°K, V_{GS} = 0 V. Curve P, 2N5270, T_C = 92°K, V_{GS} = 0 V.

Figure 3 Equivalent input noise voltage and the reciprocal of the forward transadmittance versus device temperature for p-Si (Curves A, B, D) and n-Si (Curves C, E). Curves A and D, 2N5270, V_{GS} = 0 V, V_D = 15 V. Curve B, 2N5465, V_{GS} = 0 V, V_D = 10 V. Curves C and E, 2N4416, V_{GS} = 0 V, V_D = 7 V.

Figure 4 Two ^{241}Am X-ray spectra obtained with different types of JFET. Spectrum P, p-Si (2N5270), counting time 20 minutes. Spectrum N, n-Si (2N4416). The detector was a silicon surface barrier type.

1. INTRODUCTION

Many of the recent developments* in semiconductor detector cooled preamplifiers have concerned the input junction field effect transistor (JFET), but attention has mainly been limited to a few similar n-channel types, such as the 2N4416 and the 2N3823. While the p-Ge TIXM12 has been operated successfully in liquid helium, the performance of p-Si JFET's in liquid nitrogen cryostat systems has been much inferior to that of n-Si units. Practical comparison of different types of JFET in this application requires a careful study of the various noise sources, both internal and external to the JFET structure proper. The noise due to each source varies in a different manner with the operating conditions. Achievement of the lowest noise performance for a given JFET therefore requires a careful optimisation procedure. When this is done, similar n and p-Si devices can give comparable performance, despite the lower transadmittance of p-channel units due to the lower mobility of holes compared with that of electrons.

The measurement and optimisation procedures are described in the following two sections. Section IV covers the practical application to preamplifiers which used a cooled Schottky barrier diode as a current leak path (Eberhardt 1970) so as to eliminate the high value gate leak resistor as a source of noise external to the JFET.

2. METHOD OF MEASUREMENT

The first requirement in the measurement of low input noise levels is the exclusion of extraneous noise, especially at low frequencies, by careful shielding and layout of the JFET gate circuit. Only components with the minimum of capacity and inherent noise sources can be tolerated. Even after careful cleaning the JFET case dielectric is a possible noise source (Kern and McKenzie 1970). The input stage components, including a 1 pF calibration capacitor, were mounted inside the cryostat, the JFET case temperature (T_C) being measured with a copper-constantan thermocouple. The later stages of the voltage sensitive preamplifier were attached to the outside of the cryostat. This was followed by an active filter main amplifier (shaping time constant set at 4 μs) and a true r.m.s. voltmeter.

The operating temperature of the input JFET was varied either by changing the cryostat cold finger temperature or the JFET internal power dissipation or both. The JFET case was mounted in a metal block in good thermal contact with the cryostat cold finger and so could be considered as an infinite heat sink.

3. OPTIMISATION OF JFET OPERATING CONDITIONS

The equivalent input noise voltage (e_{in}) of the JFET device itself (as

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* Elad and Nakamura 1967, 1968; Elad 1969; Goulding et al. 1969, 1970; Radeka 1969, 1970; Kern and McKenzie 1970.

distinct from JFET plus package or case and other devices connected to the gate) is a function of drain current (I_D) forward transadmittance (y_{fs}), input capacitance (C_{iss}), drain voltage (V_D), gate current (I_G) and dice temperature (T_D) (see Table 1). The properties of the epitaxial layer within which the device is constructed also affect e_{in}. In particular the type and density of trap - recombination levels, and the ionisation energy of donor or acceptor impurity levels influence the variation of e_{in} with T_D. The determination of the optimum operating conditions for the JFET and the comparison of the performance of different JFET types requires a careful examination of the variation of e_{in} with the above parameters.

TABLE 1

JUNCTION FET COMPARISON

Parameter	T_D °K	2N4416 n-Si	2N5270 p-Si
y_{fs}, μ℧	250	6,500	2,700
	130	9,200	5,500
$\bar{e}_{in}$, μV	250	0.90	5.5
	130	0.75	0.95
C_{iss}, pF	300	4	5.5
r_t, °K/W	130	280	280

The first necessary step in this optimisation procedure is the measurement of the thermal resistance (r_t) of the JFET (Ryan unpublished), so that T_D can be calculated,

$$T_D = T_C + P\, r_t \quad . \qquad \ldots(1)$$

The values of r_t (280°K/W) and P (through V_D and I_D) indicate that the difference ($T_D - T_C$) can be as large as 90°K.

The second step is the measurement of the threshold drain voltage V_T above which I_G increases rapidly due to impact ionisation in the pinched off channel (Ryan 1969). For devices with similar dimensions and epitaxial layer parameters, V_T increases through the series p - Ge, n - Si, to p - Si. Measurements on n - Si JFET's with different parameters (2N4416 and 2N5543) indicate that V_T increases

with length of the pinch region, that is, lower field in the pinch for a given V_D. It is also necessary to check the small decrease in V_T with T_D. The minimisation of e_{in} requires that $V_D < V_T$.

The third step is the study of the change of e_{in} with T_D, by varying both T_C and P. The main noise source of the ideal JFET structure is considered to be due to the thermal noise from the channel (Van der Ziel 1962):

$$e_{in,th} \propto \frac{T_D}{y_{fs}} \quad . \qquad \ldots(2)$$

Thus thermal noise decreases with T_D and with increase of y_{fs}. However this third step is complicated in at least two ways. Actual JFET's are not ideal and so noise sources other than the channel thermal noise are often dominant. For example, they may arise from unwanted impurities in the epitaxial layer into which the JFET structure is diffused. The second complication is that y_{fs} is a function of T_D and I_D so that a detailed check of Equation 2 requires a protracted series of measurements. Such measurements are not reported here.

In measuring the noise due to non-ideal sources in Si JFET's it is convenient to begin with T_C constant at values near 80°K and to measure e_{in} as P, and thus T_D, are increased. The observed changes in e_{in} can then be due only to the JFET itself and not to changes with temperature of external components. Figure 1 shows the results of such a set of measurements on 2N4416 devices from two different manufacturers. As V_D is varied, large differences in e_{in} become apparent. These are probably due to depletion region modulation noise arising from impurity trap - recombination levels (Spaulding 1968) the density of levels being considerably lower in device 1 (curve C). The plots A and B for device 4 taken under different operating conditions indicate that the peak in e_{in} occurs at a constant T_D 95°K, corresponding to the activation energy of an impurity level. The increase in e_{in} at $V_D > 10$ volts is common to both devices and is due to I_G.

A similar set of results given in Figure 2 does not show any peak due to impurity levels for the p-Si JFET between 100°K and 140°K. The difference in the high V_D values for the n- and p-channel units, at which e_{in} increases rapidly, is due to two causes, gate current and temperature increase. With the n-channel device, I_G is the dominant cause, whereas in the p-channel case T_D has the major effect. This is shown more clearly in Figure 3, where e_{in} increases more rapidly with T_D for the p-Si JFET's. The general decrease of e_{in} with T_D shown in Figure 3 is in agreement with Equation 2. The difference between e_{in} for the n- and p-Si units near 120°K is noticeably less than is to be expected from their different values of y_{fs}. This result, together with other observations on n-Si JFET's operating at low I_D and so low y_{fs} indicates that at temperatures near 120°K the optimum operating point with low capacity X-ray detectors is not necessarily that

which gives the highest y_{fs} (that is, $V_{GS} = 0$). One possible reason for this is the increase in 1/f noise at higher frequencies as I_D is increased (Craig and Sesnic 1970). Further work is needed in this area.

When e_{in} is measured for T_D below 100°K, Figures 1-3, it is found to increase (Elad 1969, Radeka 1969). This is due to the effects of de-ionisation of donor or acceptor impurity levels on carrier drift mobility (μ) and gate depletion layer width (W). This de-ionisation, or freeze-out of carriers, is due to the decrease with T_D in the separation of the Fermi level and the impurity level (Grove 1967, Sze 1969). Both μ and W increase with decrease of T_D below 300°K, well before de-ionisation becomes significant, the net increase in I_D and y_{fs} contributing to the observed decrease in e_{in} (Figure 3). The carrier mobility is determined by lattice scattering, ionised impurity scattering and at the lowest temperatures by carrier 'trapping' in impurity levels, that is, return of a carrier to a donor or acceptor level, followed by thermal release into the conduction or valence band. The net effect at lower temperatures and at the levels of doping used in JFET epitaxial layers is to cause a decrease in μ (Blakemore 1969). The de-ionisation will also accelerate the increase in W, so that decrease of T_D causes a decrease of I_D and y_{fs}. However, the increase in e_{in} is greater than is to be expected from the decrease in y_{fs} and Equation 2. The de-ionisation process is an additional fluctuation process in the carrier density not considered in the theory (Van der Zee 1962) underlying Equation 2. This process will affect the drain current fluctuations directly through the carrier density in the channel and indirectly through changes in W.

4. PRACTICAL APPLICATION

The practical application of the type of results obtained above requires the control of T_D under normal cryostat operating conditions. The difference between the cold finger temperature, near 77°K, and the optimum $T_D \approx 120$°K requires heating of the JFET. External electrical heating can introduce interference noise and complicate the cryostat mechanical design. Self heating of the JFET is more convenient. The higher values of V_D allowed with the 2N5270 p-Si devices make it possible to optimise T_D with r_t unchanged. For the 2N4416 n-Si JFET the restriction of V_D to values below 10 V, and of I_D to relatively low optimum values, makes it necessary to increase the effective value of r_t. It can be increased from 280 to 870°K/W by moulding the JFET (and the cooled diode leak (Eberhardt 1970)) into the top of a short epoxy column, which is fixed to the cold finger. For n-channel devices with different values of r_t, V_T and optimum I_D (for example TIXS 35) this increase of the effective r_t may not be necessary.

Two spectra obtained with p- and n-Si JFET preamplifiers are given in Figure 4. They show that comparable resolution (500 eV pulser is obtained when the

operating conditions are optimised. The resolution was limited by the detector. Long counting times did not degrade the resolution, indicating the long term stability of the voltage sensitive mode of operation. The electronic system resolution without a detector connected (no added capacity) was below 300 eV (FWHM Si) for both p- and n-Si JFET's. It is probably limited by JFET and diode case dielectric noise (Kern and McKenzie 1970). The overhead cryostat used can also be a source of vibration noise due to bubbling of liquid nitrogen.

5. CONCLUSION

The general need for a detailed optimisation procedure when comparing the performance of different JFET's in low noise preamplifier input stages has been demonstrated for the particular case of n- and p-channel Si devices. The relative density of impurity levels in the epitaxial layers of devices with the same type number can be readily detected when the device temperature is varied by varying the dissipation. The fact that comparable performance can be obtained from n- and p-channel JFET's differing considerably in y_{fs} indicates that at the optimum temperatures channel thermal noise is not the only JFET limitation to high resolution.

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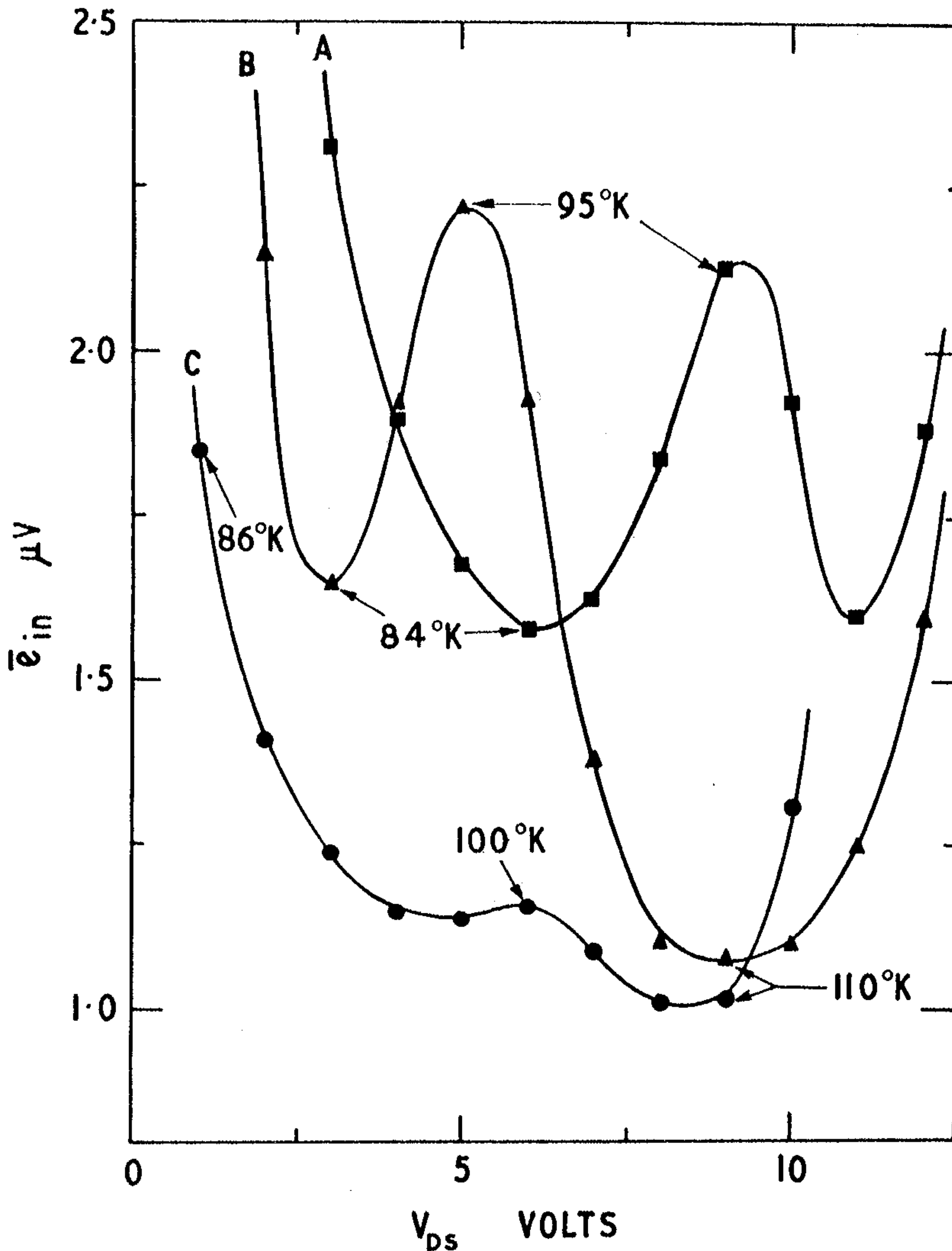

FIGURE 1. EQUIVALENT INPUT NOISE VOLTAGE VERSUS DRAIN VOLTS FOR TWO 2N4416's FROM DIFFERENT MANUFACTURERS. The values marked are estimated device temperatures (r_t = 280°K/W).
Curves A and B, device 4, T_C = 72°K; A, V_{GS} = −1 V; B, V_{GS} = 0 V.
Curve C, device 1, T_C = 84°K, V_{GS} = 0 V.

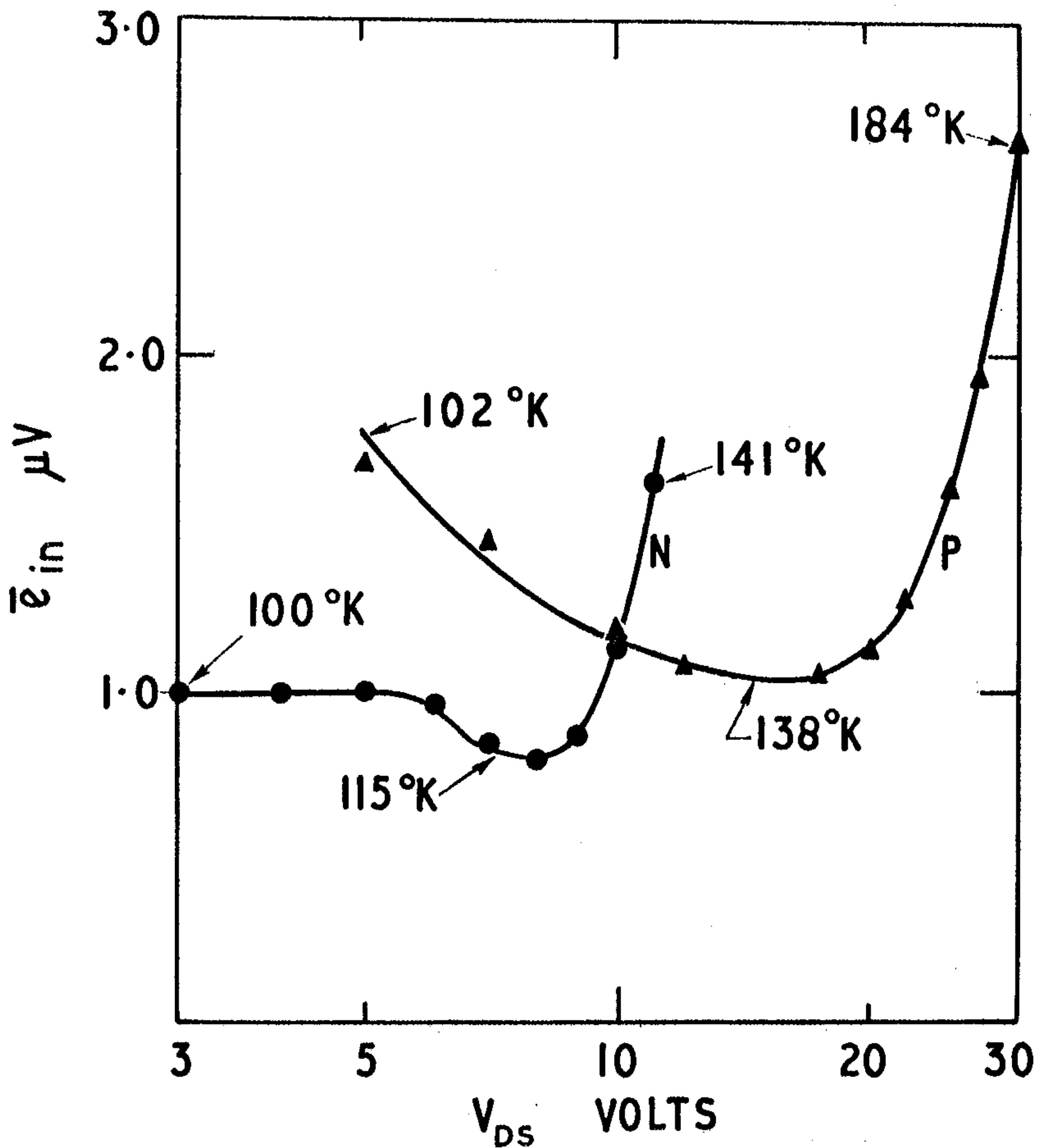

FIGURE 2. EQUIVALENT INPUT NOISE VOLTAGE VERSUS DRAIN VOLTS FOR p-Si (CURVE P) AND n-Si (CURVE N) JFET's.
Curve N, 2N4416, $T_C = 93°K$, $V_{GS} = 0$ V.
Curve P, 2N5270, $T_C = 92°K$, $V_{GS} = 0$ V.

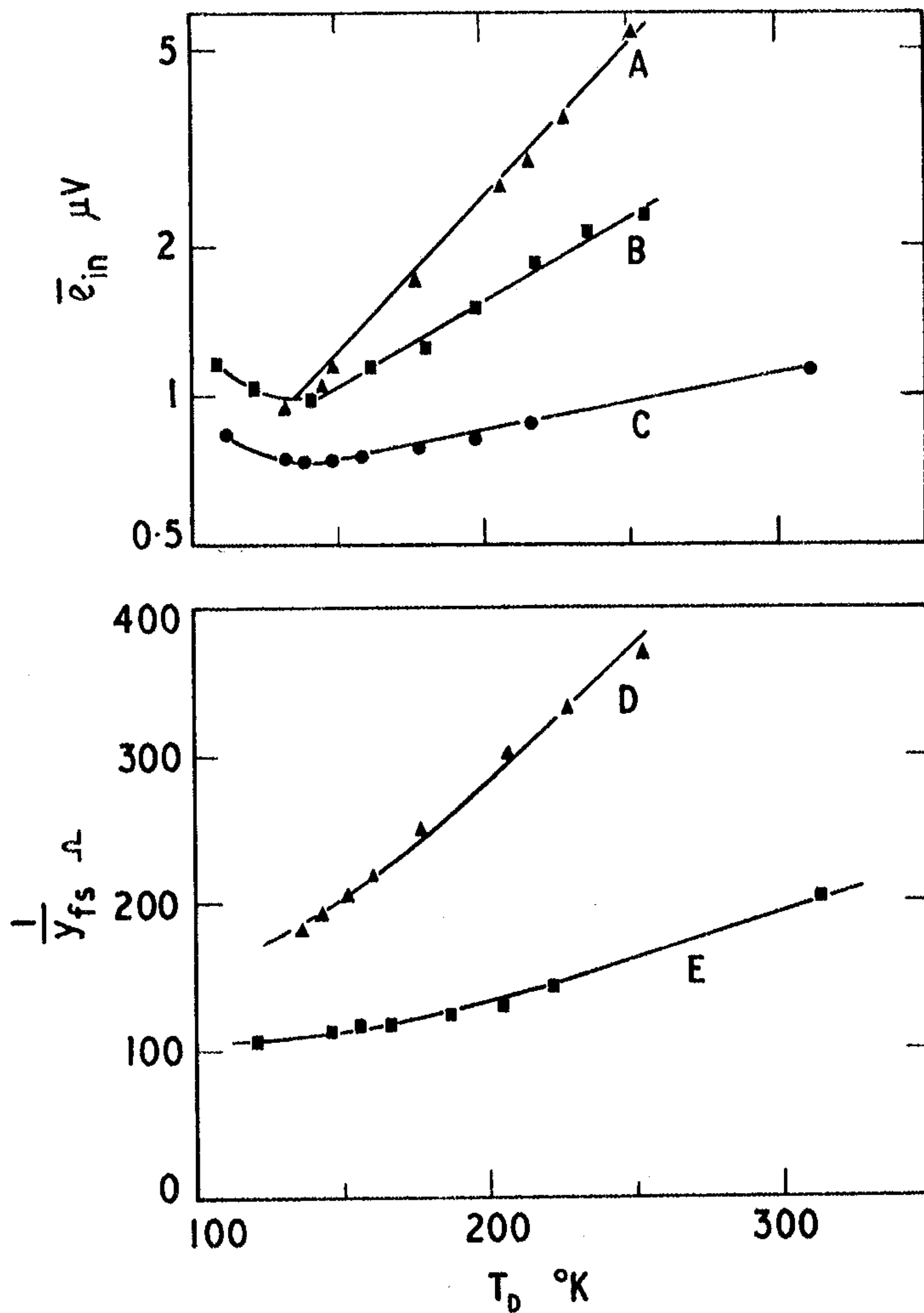

FIGURE 3. EQUIVALENT INPUT NOISE VOLTAGE AND THE RECIPROCAL OF THE FORWARD TRANSADMITTANCE VERSUS DEVICE TEMPERATURE FOR p-Si (CURVES A, B, D) AND n-Si (CURVES, C, E).
Curves A and D, 2N5270, $V_{GS} = 0$ V, $V_D = 15$ V.
Curve B, 2N5465, $V_{GS} = 0$ V, $V_D = 10$ V.
Curves C and E, 2N4416, $V_{GS} = 0$ V, $V_D = 7$ V.

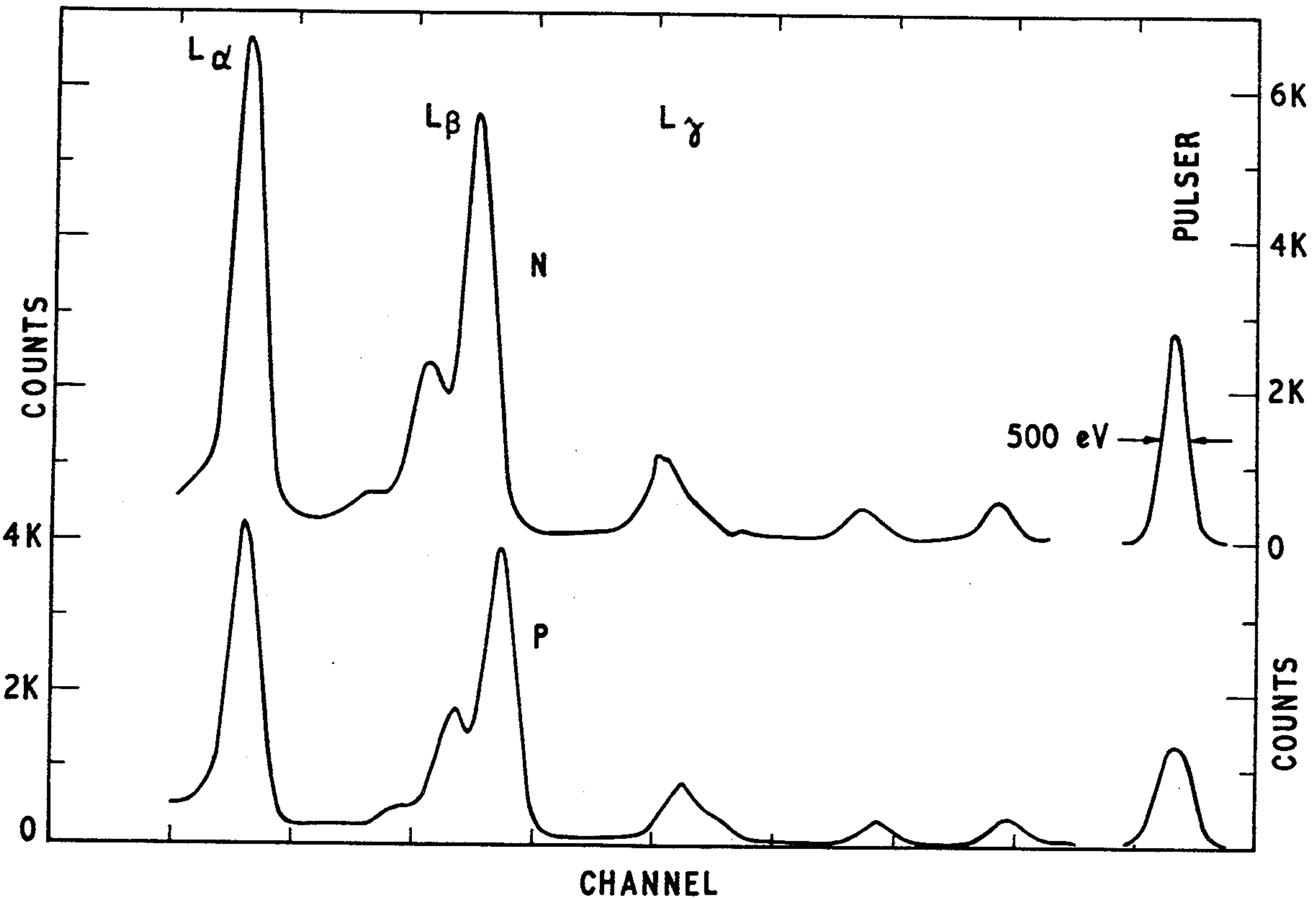

FIGURE 4. TWO ^{241}Am X–RAY SPECTRA OBTAINED WITH DIFFERENT TYPES OF JFET. Spectrum P, p-Si (2N5270), counting time 20 minutes. Spectrum N, n-Si (2N4416). The detector was a silicon surface barrier type.