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ABSTRACT

Rapid thermal annealing of neutron transmutation doped silicon wafers is shown to be an alternative to the normal furnace annealing procedure. A prototype incoherent light, rapid thermal annealing, 4.5 kW furnace has been constructed which can raise the temperature of 75 mm diameter silicon wafers to 1120°C. Successful annealing is demonstrated by comparing the resistivities of the wafers with those from furnace annealed standards. Deep level transient spectrometry has been performed to show that there are no electrically active deep level impurities present. Although there is evidence for crystalline slip, it does not appear to affect the results.

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ANNEALING; CRYSTAL DOPING; ELECTRIC CONDUCTIVITY; FURNACES; IRRADIATION; SILICON; TRANSMUTATION; VERY HIGH TEMPERATURE

EDITORIAL NOTE

From 27 April 1987, the Australian Atomic Energy Commission (AAEC) is replaced by Australian Nuclear Science and Technology Organisation (ANSTO). Serial numbers for reports with an issue date after April 1987 have the prefix ANSTO with no change of the symbol (E, M, S or C) or numbering sequence.

CONTENTS

1. INTRODUCTION

Neutron transmutation doped silicon (NTD-Si) has become a technologically important material in the last decade. The uniform phosphorus concentration produced by neutron absorption and consequent transmutation in silicon makes NTD-Si very suitable for large high-power devices such as thyristors. An undesirable consequence of neutron irradiation is the damage to the crystal lattice. This damage is usually annealed on whole ingots in an inert-atmosphere furnace at temperatures above 700°C, for times of an hour or more. Device manufacturers would judge the success of the anneal first by the resistivity attained, and second by the associated minority carrier lifetime. The annealing procedure involves a number of factors such as neutron dose and energy spectrum, and oxygen concentration in the initial material. Irradiation of float-zoned(FZ) Si in a nuclear reactor having a well-thermalised neutron spectrum is the preferred combination of material and neutron source.

Rapid thermal annealing (RTA) is a well established technique for the annealing of radiation damage produced by ion implantation. Annealing times are in the range 10^{-8} to 10^{2} s, which is too short a time for significant diffusion of the implanted species, or for contamination by undesirable deep-level impurities. Most RTA techniques involve heating of the whole wafer and annealing by solid phase epitaxy. Incoherent light sources are probably the most common of these techniques and RTA lamp annealing is becoming accepted in industrial processing.

Through what may have been an oversight, the RTA process has not been assessed as an annealing technique for NTD-Si. Since RTA is a bulk heating technique, and since the radiation damage associated with NTD-Si is, in general, far less severe than that produced by ion implantation, annealing should be successful. It should, however, be pointed out that the two irradiation processes produce different types, as well as different densities of defects. An obvious advantage of the successful rapid thermal annealing of NTD-Si would be the reduced possibility of contamination. Only one reference to the annealing of NTD-Si by an RTA technique has been found in the literature. This is the work of Pollard *et al.* [1985] who, with a scanning electron beam system, found that annealing occurred for times as short as 30 s provided that the temperature was above 800°C. This technique has the practical disadvantage that it is carried out in vacuum.

A number of experiments have been carried out to demonstrate that RTA can readily be used to anneal NTD-Si wafers. In this work, incoherent light is used to show that annealing occurs. A prototype RTA furnace was constructed which provides 4.5 kW for up to 99 s. In this furnace the temperature of 75 mm diameter wafers was raised to about 1120°C. Resistivity measurements and deep level transient spectrometry (DLTS) were then used to find if annealing was complete. Deep level transient spectrometry is a more revealing secondary analysis technique than the measurement of minority carrier lifetime. The correlation between lifetime and DLTS measurements is not well established but trap densities and cross-sections are obviously important.

The results of a comparison of wafers annealed by RTA and those processed by conventional furnace annealing (FA) are also reported. There are temperature gradients within the RTA furnace which cause crystalline slip in the larger wafers. However, the results indicate that this slip has negligible effect on the resistivity and DLT spectra.

2. EXPERIMENTAL

2.1 RTA Incoherent Lamp Furnace

The heart of the RTA furnace consists of two horizontal arrays of (linear) tungsten-halogen lamps, one above the other. Each lamp has a useful filament length of 7.5 cm, dissipates 0.5 kW, and is separated from its neighbours by a 1.5 cm gap (filament to filament). The bottom array consists of five lamps in parallel, the top of four; there is a gap of about 3.0 cm between the two arrays (filament to filament) in which the sample is held. The top array is displaced sideways by 0.75 cm (half the inter-filament spacing), see **figure 1**. The wafer is mounted horizontally on two quartz rods so that when in position it is equidistant from the two arrays. The lamp arrays are surrounded by a palladium-coated, stainless steel reflector.

The power to the arrays (240 V a.c.) is controlled so that the lamps can be switched on for times in the range 0 - 99 s. A 75 mm wafer attains a peak temperature of 1120°C at its centre. There are significant temperature gradients in the furnace, as is shown in **figure 1**.

2.2 NTD Silicon Wafers

The wafers were irradiated at Lucas Heights in HIFAR, a DIDO class, 10 MW heavy-water moderated and cooled reactor. The neutron spectrum in the core is well thermalised, having a cadmium ratio of about 1000. The wafers were given doses in the range 4 - 8 × 10^{17} cm^{-2} thermal neutrons which resulted in final resistivities of 40 - 60 Ω.cm. With one exception the initial resistivities were greater than 1.5 kΩ.cm and the material was n-type FZ. All of the material examined had a <111> orientation. Resistivity details are given in **table 1**.

The resistivity results were compared with control wafers which were irradiated simultaneously but annealed in the standard manner. The standard furnace annealing cycle is 2 h at 800°C, which was established on the basis of earlier resistivity and DLTS measurements.

Wafers to be annealed by the RTA technique are etched to remove possible radioactive contaminants and have a bright specular finish. To anneal a wafer, the furnace is usually run at full power (4.5 kW) for 99 s. The temperature rises rapidly in the first 30 s and then tends to saturate. The fall time is approximately exponential and the temperature drops to half its maximum value in about 20 s. The furnace atmosphere is the same as that in the laboratory.

Resistivity measurements were made after lapping the surfaces with a 1200 grade SiC grit and water slurry on glass. A co-linear four-point probe was used and all measurements were normalised to 23°C, at which temperature resistivity standards were available to calibrate the probe system. Provided that the initial resistivity is high, for example 1.5 kΩ.cm, the final resistivities of wafers receiving the same neutron dose can be directly compared.

After the resistivity measurements were completed, the slices were examined twice. One examination involved the use of a surface decorating etchant to look for crystalline slip; the recipe (the Wright etch) given by Jenkins [1977] was used. The second examination was capacitance DLTS of 8 mm x 8 mm sections with Au blocking contacts and Al ohmic contacts.

3. RESULTS

The first batch of wafers were quite small in diameter (32 and 35 mm) and each pair was cut from a single larger wafer. Once it was established that these were being successfully annealed, the wafer diameter was increased to 75 mm, the maximum for the furnace, and the pairs consisted of separate wafers with different initial resistivities. There was no evidence for slip on the smaller wafers and it was possible to reduce their annealing time from 99 to 60 s (**table 1**). The initial resistivities supplied by the manufacturer (Komatsu Electronic Metals) apply strictly to the centre of the original wafer. A sample of magnetic Czochralski (MCZ) Si with a low initial resistivity was examined but it was not obviously different from the FZ material. It must be appreciated that associated with each measurement of resistivity is an experimental error; in the present case, one standard deviation is typically 0.5 per cent.

Once the wafer diameters were increased to 75 mm, evidence for crystalline slip was found using the Wright etch method. **Figure 2** shows slip patterns characteristic of <111> orientation on a 75 mm wafer. A slice along a diameter has been removed to provide DLTS samples. However, the resistivity results and DLT spectra did not appear to be influenced by this slip. With regard to the DLT spectra, this observation is in contrast to the findings of Ransom *et al.* [1986]. However, these authors annealed unirradiated material, 100 Ω.cm, <100>, n-Si, for only 10 s. When the wafer diameter was reduced from 75 to 50 mm, the amount of slip was also reduced, and confined to the wafer perimeter.

4. DISCUSSION AND CONCLUSIONS

The results show that RTA is a suitable technique for annealing NTD-Si wafers. However, it is not likely to be useful for annealing ingots. It could be applied as one step in an industrial process provided that wafers were to be annealed. For this reason it may be of some interest to discuss our procedures.

To calibrate HIFAR for commercial NTD-Si irradiations, and to provide checks of neutron flux and fluence during such irradiations, many NTD-Si wafers were treated by the standard FA method. The various steps from irradiation to resistivity measurement are shown in **table 2**. For comparison, the steps taken for RTA processing are also shown.

Step 2 is basically a precautionary measure and, provided that the wafers are held long enough after irradiation, may not strictly be necessary. This step will, however, remove both active and non-active surface contaminants. Because of the short time involved, this step is much less important for RTA. In fact, it is probably superfluous.

For the standard FA process, step 3 is very important; it is undertaken to ensure that such contaminants as Na and Au from step 2 are not left on the surface of the wafers. This step is not necessary for the RTA process so there is a consequent saving in time and chemicals. A much shorter annealing time (step 4) is required for RTA processing. The standard procedure at this laboratory (FA) is to allow the wafers to cool down with the natural time constant of the furnace. It is therefore, several hours before a FA wafer can be handled again, but only a few minutes need to elapse before an RTA wafer can be handled.

Because of the higher probability of contamination with furnace annealing, ingots are preferred to wafers. However, if the RTA of NTD-Si was adopted as a step in a production process, it might be worthwhile considering the neutron irradiation of wafers instead of ingots. This could have an economic benefit. At present, a considerable fraction of an NTD-Si ingot is lost in the slicing process; this represents an inefficient use of the reactor. Of course, there would undoubtedly be far more serious packaging and handling problems associated with the irradiation of wafers which could negate any advantage.

The temperature gradients in the prototype RTA furnace are sufficiently significant to cause crystalline slip in larger wafers with areas that are a significant fraction of that of the furnace. However, the resistivity and DLTS results do not seem to be affected. Nevertheless, although some slip may be tolerated in quality control wafers (as in the present case) it may be desirable to have slip-free material in a production run. Improvements to the reflectors, and control over the decay of the thermal pulse, should remove the slip. The RTA furnace could readily be scaled up to handle larger wafers, for example, 100 and 125 mm.

5. ACKNOWLEDGEMENTS

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Ransom, C.M., Sedgwick, T.O., Cohen, S.A. [1986] - In *Rapid Thermal Annealing* (ed. Sedgwick, T.O., Seidel, T.E., Tsaur, B.-Y.) *Mater. Res. Soc. Symp. Proc.*, 52:153.

NOTES

TABLE 1
RESISTIVITY (ρ) AND DLTS RESULTS FROM RTA AND FA WAFERS

The initial resistivity of the wafers is given in brackets after the wafer identification. A clean DLT spectrum is one in which no majority or minority peaks are observed.

Base Material	Ident.	RTA Time @ 4.5 kW	Wafer $\phi \times w$	ρ (RTA) Ω.cm	ρ (FA) Ω.cm	DLTS
100 mm ϕ FZ	WA-12 (1720)	60 s	35 × 2.5	44.3		clean
same wafer	WA-12 (1720)		35 × 2.5		44.7	
125 mm ϕ MCZ	A0054 (646)	60 s	32 × 2.0	43.7		clean
same wafer	A0054 (646)		32 × 2.0		44.1	
75 mm ϕ FZ	A0116 (2950) *	100 s	75 × 1.0	50.8		clean
similar wafer	AO117 (2050)		75 × 1.0		53.1	
75 mm ϕ FZ	A501 (2910)	100 s	75 × 2.0	41.1		clean
similar wafer	A500 (2870)		75 × 2.0		41.7	
75 mm ϕ FZ	A505 (1735)	100 s	50 × 2.0	39.4		clean
similar wafer	A509 (1990)		50 × 2.0		39.9	

* = broken, ϕ = diameter, w = thickness, ρ = resistivity

TABLE 2
COMPARISON OF A PROCESS USING RTA WITH ANOTHER USING CONVENTIONAL FA

Step	Conventional Process (FA)	New Process (RTA)
1	irradiation	irradiation
2	remove radioactive traces	remove radioactive traces
3	clean wafer surfaces	not applicable
4	FA	RTA
5	lap	lap
6	measure resistivity	measure resistivity

NOTES

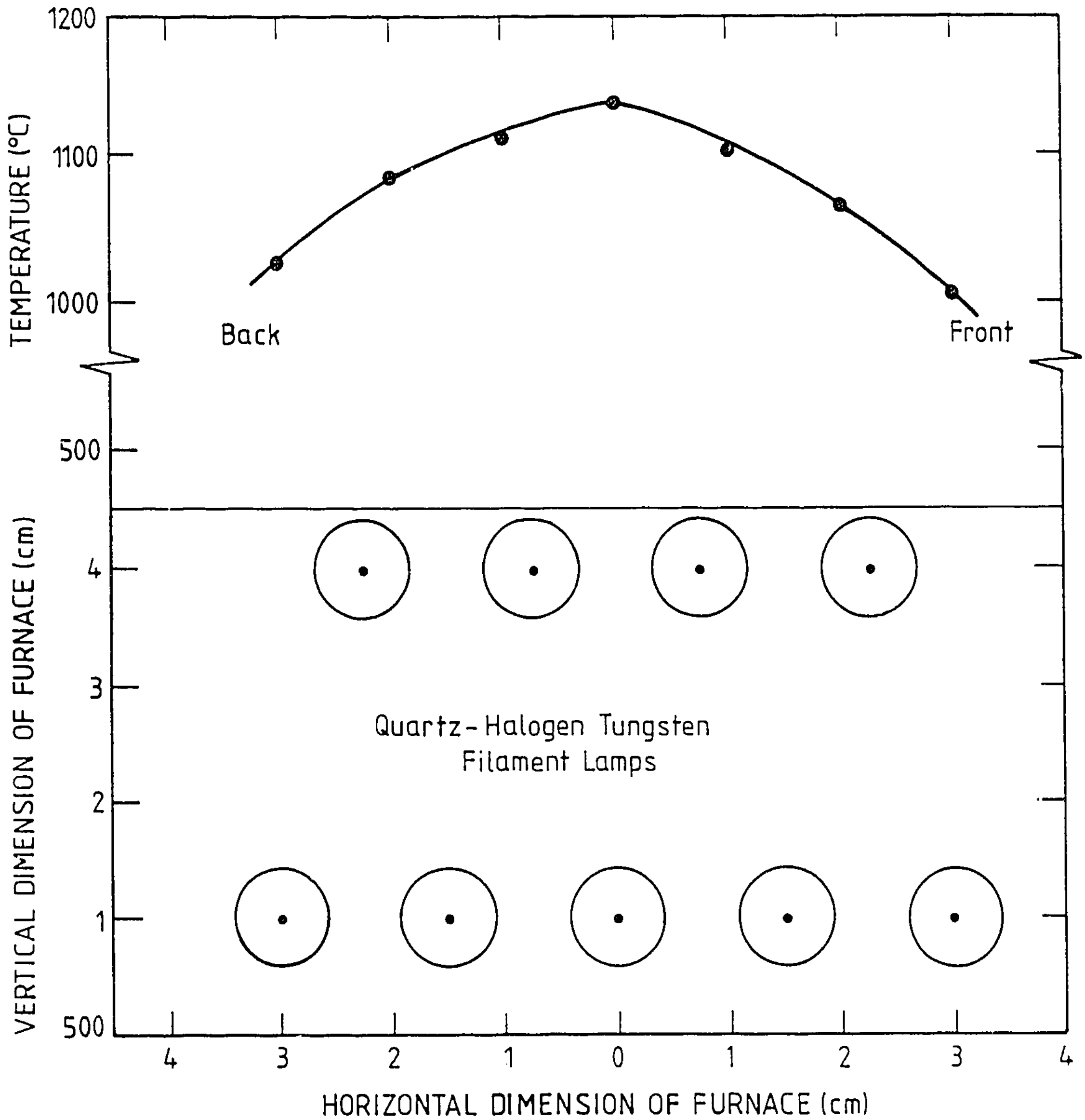

Figure 1 Temperature distribution in the prototype incoherent light, rapid thermal annealing furnace. The distribution is approximately radially symmetric. A cross section of the furnace is also shown (viewed along the lamp axes).

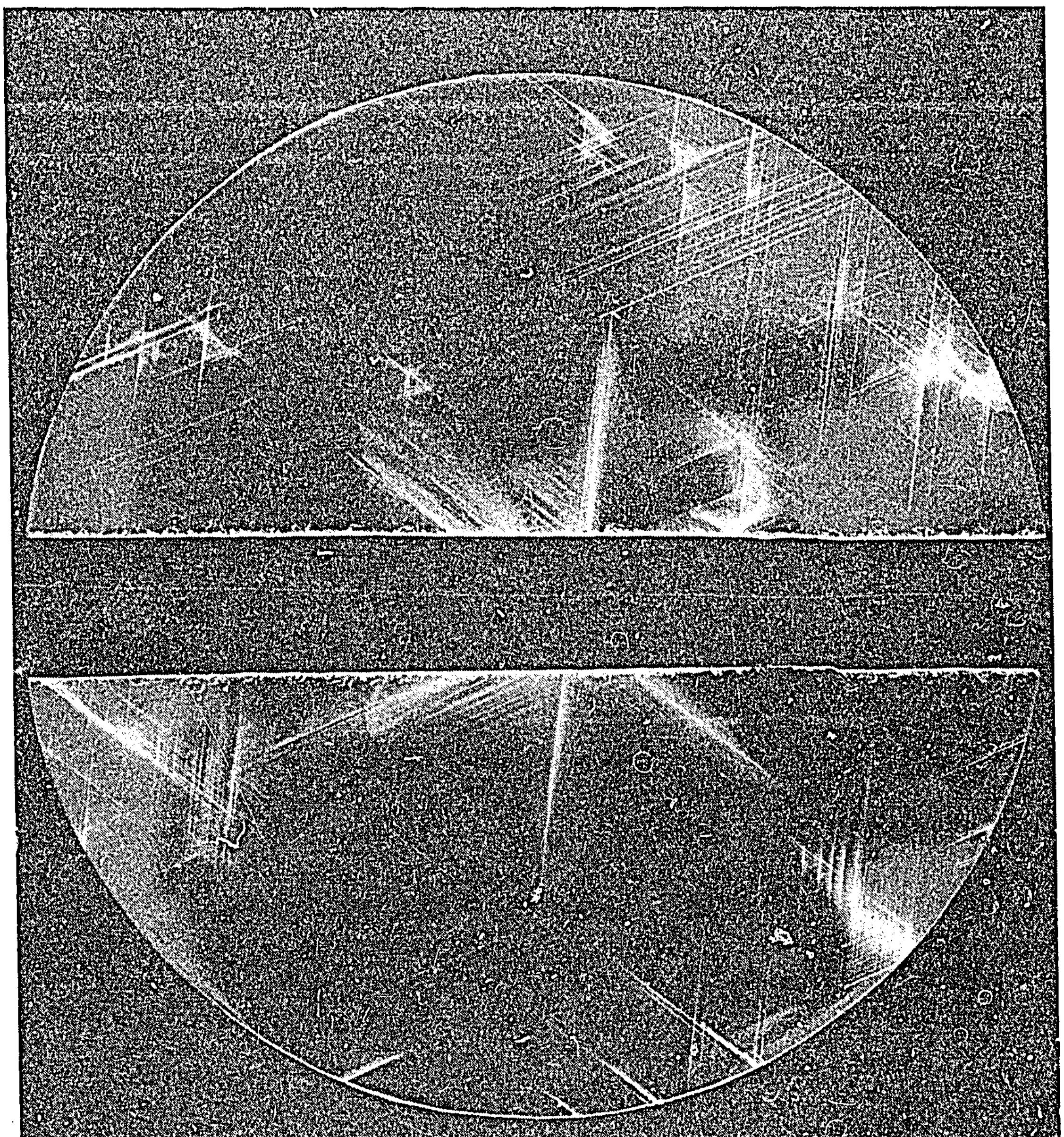

Figure 2 Slip patterns delineated on a 75 mm diameter <111> orientated Si wafer. The material along the diameter has been removed to provide samples for DLTS.