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PULSE HEIGHT ANALYSIS USING A PDP-15 COMPUTER

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ABSTRACT

The use of a PDP-15 computer in a pulse height analysis system is described. Both the analogue-to-digital converter and the cathode ray oscilloscope display have direct access to the computer memory and hence the only programming required for their control is the setting up of status words.

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continued ...

CONTENTS (continued)

1. INTRODUCTION

Pulse height analysis is the technique applied to data consisting of a series of voltage pulses whose amplitudes are proportional to a parameter being studied. The parameter range is divided into a number of channels and the arrival of each pulse is recorded by adding one to the count in its corresponding channel. A graph of channel contents against channel number is a spectrum of the incoming pulses.

Modern pulse height analysers are digital instruments having three essential elements: an analogue-to-digital converter, a memory, and a cathode ray oscilloscope display. Output devices such as pen plotters and printers can be included.

The considerable reduction in the price of small computers has now made it an attractive proposition to use them as controlling devices in pulse height analysis systems. The analogue-to-digital converter and the display are peripheral devices to the central processor and segments of the computer memory are assigned for accumulating data. Operation of the external devices is coordinated in a general pulse height analysis program but programs can be added for specialised data processing tasks in particular applications.

This report describes a pulse height analysis system based upon a PDP-15 computer[1]. The system makes use of direct memory access (Reference 2, pp.3-4) for both the analogue-to-digital converter and the display, which consequently means a very low dead time for the conversion of incoming data and a clear non-flickering display which is unaffected by the rate of data entry.

2. EQUIPMENT RESUMÉ

2.1 Analogue to Digital Converter (A.D.C.)

A Nuclear Data Corporation 2200 series instrument[3] is used, capable of 4096 channel (12 bit) conversion. Its 50 MHz clock rate gives a maximum conversion time of approximately 82 microseconds but smaller ranges can be selected using front panel switches, hence reducing the conversion time.

2.2 Display Cathode Ray Oscilloscope (C.R.O.)

The C.R.O. is a BWD Electronics instrument[4] which has an 8 cm x 10 cm screen. The X-axis is operated by a 12 bit (4096 channel) digital to analogue converter while the Y-axis has a 10 bit (1024 channel) converter. The interface scales the data to give a full screen display for all ranges of channel number but extra magnification is available from the C.R.O. controls.

2.3 The Computer

The PDP-15 computer is an 18 bit word length machine with a one microsecond

cycle time. It has 8192 words of memory. Direct memory access is provided for both single cycle and multicycle operations. A teletype ASR33 is used for typing in commands and for printing spectra and other data at ten characters per second. This unit can also be used to punch and read perforated paper tape.

2.4 A.D.C. Interface

The A.D.C. converts the amplitude of each incoming pulse to a binary number, and the size of this number determines the channel to which the incoming pulse is to be assigned. The task of the interface between the computer and the A.D.C. is to add this number to a base address and present the result to the computer. The computer adds one to the contents of the memory address to which this number refers. The important feature of this interface is that it operates independently of the program by accessing the memory directly. This means that the rate of conversion is limited only by the A.D.C. speed and not by the program speed.

The interface has a register which contains the necessary information to assign a data region and to allow or inhibit A.D.C. operation. This register is loaded with a status word from the computer which is set up by the program from information that the user types in at the keyboard. The computer translates commands and parameters into a suitable status word for the A.D.C. interface. The structure of the A.D.C. status word is given in Section 3.

2.5 C.R.O. Interface

The function of the display is to provide a dynamic picture of the accumulation of counts into channels. The number of counts for each channel (Y-axis) is plotted against channel number. Vertical lines whose location can be set to coincide with a given channel are provided as markers to identify peaks.

The C.R.O. interface selects the channel to be displayed, requests the contents of this channel from the computer and using two digital-to-analogue converters moves the dot on the C.R.O. screen to the correct position. This interface has two registers which contain the necessary information to set up a display. The only programming required for the display is the setting up of the status words. Once this is done, the display is generated automatically by direct memory access independently of the program. The status words are set up from information typed in by the user, their structure being that given in Section 4.

3. A.D.C. OPERATION

The 18 bits of the A.D.C. status word are assigned as in Table 1. It is set up in the PDP-15 accumulator by program and transferred to the A.D.C. control register by the instruction IOT2004.

TABLE 1 - A.D.C. STATUS WORD

BIT 0 — ENABLE/DISABLE A.D.C.

BIT 1 — ENABLE/DISABLE OVERFLOW

BITS 5	6	7	8	9	10	11	BASE ADDRESSES
	0	0	0	0	0	0	4096 CHANNELS
		0	0	0	0	0	2048
			0	0	0	0	1024
COMPLEMENT				0	0	0	512
OF					0	0	256
BASE ADDRESS						0	128
							64

BITS 12	13	14	15	16	17	RANGE MASKS
0	0	0	0	0	0	4096 CHANNELS
1	0	0	0	0	0	2048
1	1	0	0	0	0	1024
1	1	1	0	0	0	512
1	1	1	1	0	0	256
1	1	1	1	1	0	128
1	1	1	1	1	1	64

Bit 0 is 1 when the A.D.C. is enabled to take data and 0 when it is disabled. Bit 1 is 1 when an interrupt to the mainline program is allowed on the overflow of a channel. It is 0 when such overflows are to be ignored.

Any part of the computer memory can be assigned to take data and this assignment is made by means of the base address in bits 5 to 11. For a given size of memory the larger the number of channels per region, the fewer is the number of available regions, and hence the smaller the number of base addresses available for larger numbers of channels.

Bits 12 to 17 contain a coding of the region size. For example 111000 is the coding for 512 channels and this means that counts are accumulated in the following memory region:

(base address) to (base address + 512) .

A data word received from the A.D.C. that is greater than 512 is ignored. However, if the front panel region size switch on the A.D.C. is set to 512 then dead-time is reduced because out of range data is excluded. The following IOT (Reference 2, pp.4-1) pulses from the PDP-15 operate the A.D.C. interface.

IOT 2001	Skip on Overflow Flag
IOT 2002	Clear Overflow Flag
IOT 2004	Load A.D.C. Status word.

4. DISPLAY OPERATION

A number of parameters are needed to set up a display. These are:

1. Number of channels (X-axis range).
2. Maximum count (Y-axis range).
3. Data region starting address.
4. Marker addresses.

These parameters are supplied to the display interface by the loading of two status words SW1 and SW2. Bits 0 to 3 of SW2 determine the mode, and the meanings of the remaining parameters in the status words depend on which of the mode bits is set. Table 2 sets out the status words for operating the C.R.O. in the three modes, Display, Mark and Set.

TABLE 2 - DISPLAY STATUS WORDS

DISPLAY MODE

	BITS 0-3	BITS 4-17
SW1	Y-shift	Region Starting Address
SW2	Mode Register (Bit 0 = 1)	X-range

MARK MODE

	BITS 0-3	BITS 4-17
SW1	Zero	Zero
SW2	Mode Register (Bit 1 = 1)	Marker Address

continued ...

TABLE 2 (continued)

SET MODE

	BITS 0-3	BITS 4-17
SW1	Y-shift	Y-data Address
	Mode Register (Bit 3 = 1)	X-data

The following IOT pulses from the PDP-15 operate the display interface:

IOT 2101	Skip on Overflow Flag
IOT 2106	Load Status Word 1
IOT 2121	Enable Overflow Flag
IOT 2126	Load Status Word 2 .

4.1 Display Mode

Mode register bit 0 is set to 1 to give this mode. It results in a histogram display automatically generated by the C.R.O. interface with channel number along the X-axis and channel contents from the computer memory along the Y-axis. The number of channels to be displayed is set by placing a code in bits 6 to 17 of SW2. The codes are shown in Table 3.

TABLE 3 - DISPLAY RANGE WORDS

BITS 6 to 17	NO. OF CHANNELS
7777_8	4096
7776_8	2048
7774_8	1024
7770_8	512
7760_8	256
7740_8	128
7700_8	64
7600_8	32

Bits 4 to 17 of SW1 give the starting address within the computer memory for the data to be displayed. Each successive memory location is the next energy

channel and the contents are the number of counts for that energy channel.

Bits 0 to 3 of SW1 give the Y-axis shift. The 18 bit word in the PDP-15 allows a maximum count per channel of 262,143. By left-shifting this word, the maximum count displayed is halved for each shift. The effect of this is to magnify the Y-axis display by two for each shift. The following Table shows the setting of the Y-shift register for given Y ranges.

TABLE 4 - Y-SHIFT REGISTER SETTINGS

SHIFT	MAX. COUNTS/CHANNEL	SHIFT	MAX. COUNTS/CHANNEL
0000	2^{18}	1000	2^{10}
0001	2^{17}	1001	2^{9}
0010	2^{16}	1010	2^{8}
0011	2^{15}	1011	2^{7}
0100	2^{14}	1100	2^{6}
0101	2^{13}	1101	2^{5}
0110	2^{12}	1110	2^{4}
0111	2^{11}	1111	2^{3}

4.2 Mark Mode

Mode register bit 1 is set to 1 to give the mark mode in which a vertical line of dots is drawn on the screen. There is only one parameter to be varied, the X-position of the marker. This is placed in bits 5 to 17 of SW2: SW1, being irrelevant in mark mode, is set to zero. This is done twice to give two markers, or repeated if further markers are required.

4.3 Set Mode

This mode gives a single point on the C.R.O. screen corresponding to X and Y values from the program. Such a mode allows the generation of miscellaneous displays by program rather than automatically as in the case of the display and mark modes. It could for example be used to draw alphameric characters on the screen for labelling peaks.

Mode register bit 3 is set to 1 to give the set mode. Bits 5 to 17 of SW1 contain the address of the Y-axis value in the computer memory, while bits 0 to 3 contain the shift applied to this Y-value as in Table 4. Bits 5 to 17 of SW2 contain the actual X-axis value. When displaying in set mode the program must load status words for every point. But in certain cases it may only be necessary to change SW2 each time because the address of the Y-value in SW1 is automatically

incremented after the point is displayed.

4.4 C.R.O. Selection

Bit 4 of SW1 set to 0 or 1 is used to select two channels for Z intensification. This means that the same interface can be used to display two different regions on separate cathode ray oscilliscopes. The X and Y connections are common to both but the Z is only intensified on the C.R.O. that is selected by bit 4.

5. PROGRAMMING FOR THE DISPLAY CONTROL AND A.D.C.

The usual display for pulse height analysis consists of a histogram and two markers. Firstly the status words for the histogram are loaded. This starts the automatic generation of the histogram and the computer is left free to perform any background tasks such as printout. When the histogram has been fully displayed, that is, when all the channels have appeared on the screen, a flag is set which interrupts the computer. The computer then loads the status words for the first marker. When the marker has been fully displayed, the flag is set again and the computer loads the status words for the second marker. The flag is set at the completion of the second marker and the computer loads once again the status words for the histogram because the C.R.O. has to be continuously refreshed. The time between the display of each point is 20 microseconds so as an example a 1024 channel spectrum plus two markers, each of 64 points would take a total of 0.025 seconds to generate, therefore this display would be refreshed at a rate of approximately 40 times per second.

The user has a number of ways of operating the A.D.C. First he may wish to have data collection for a given interval of time whereupon the programs will measure the interval using an internal clock and disable the A.D.C. at the desired time. Secondly, he may wish to terminate data collection when a channel overflows; this is the situation where the channel overflow interrupt is enabled. Thirdly, he may observe the spectrum on the C.R.O. and terminate data collection manually by typing in a command on the teletype console.

6. DESCRIPTION OF A.D.C. INTERFACE CIRCUIT

The symbols used in the circuit diagrams are given in Figure 1 and the symbol nomenclature is in Figure 2.

Figure 3 illustrates the standard method of generating input-output transfer pulses from the PDP-15 bus and also multiplexing to the data break facility (Reference 2, pp.4-19). The base address and mark registers are shown in Figure 4. IOB05 to IOB11, input-output bus bits 5 to 11, are the base address bits and IOB12 to IOB17 contain the mask whose operation is described in Section 3. To the right of the figure are the gating circuits which inhibit the memory increment, firstly if an error condition in the A.D.C. is indicated by the signal ALT(4), or secondly,

if the data is out of range of the mask. These conditions cause a pulse on the line ABORT which simply resets the A.D.C. without a data channel request being made.

Figure 5 shows the layout of input-output cables and Figure 6 the card allocation.

7. DESCRIPTION OF DISPLAY INTERFACE CIRCUIT

Figure 7 shows the data break multiplexing circuit and the mode register and Figure 8 shows the device selectors for input-output transfer pulses (Reference 2, pp.4-24). The display and mask flip-flops in the mode register are reset by overflow pulses which indicate the completion of a display or mark cycle. These pulses also set the interrupt flag.

The register loaded from IOB06 to IOB17 in Figure 9 is the range register in display mode and is the X-position register in both marker and set modes. The lower register is connected to the X-axis digital-to-analogue converter and in the case of the display mode is incremented by each data channel transfer. This increment is 1, 2, 4, 8, etc. depending on the range set in the upper register. The overflow from the lower register sets the overflow flag. In mark mode the lower register is loaded from the upper register and then does not vary.

The address and Y-axis shift registers are shown in Figure 10. After each data channel transfer the address register is incremented by one and the Y-axis shift register is loaded into a counter. In mark mode the addresses are not needed and this register is connected to the Y-axis digital-to-analogue converter to give a vertical line on the C.R.O. The overflow on bit 11 sets the overflow flag. Also connected to the address register is a one-shot which triggers at every sixteenth increment and suspends the display for several clock pulses. This leads to the brightening of every sixteenth channel by repeated intensifications of the one point. Hence the display is divided into sixteen point segments for easier inspection.

The Y-axis data register is shown in Figure 11. At each data channel transfer, data from the memory location specified in the address register is loaded and then left-shifted. The number of shifts is determined by the number of counts obtained from the Y-axis shift register, Figure 10. In display and set mode the Y-axis data register is connected to the Y-axis digital-to-analogue converter.

Figure 12 shows the digital-to-analogue converters for the X and Y-axis and also the Z-axis intensification one-shot. The one-shot is triggered after the final shift has been applied to the Y-axis data. (Note that it is also triggered by the clock pulse during the brightening of every sixteenth channel.) The intensification pulse is gated onto one of two paths by the flip-flop loaded from IOB04 for the possible operation of two C.R.O. displays. Figure 13 shows the input-output wiring layout and Figure 14 the card allocation.

8. CONCLUSION

A pulse height analysis system has been successfully implemented using a PDP-15 computer. Direct memory access for both the analogue-to-digital converter and the cathode ray oscilloscope display has led to low dead times for data conversion and minimal interaction between data conversion rate and display quality.

Because only a small amount of the processor time is involved in the servicing of the requirements of a single pulse height analysis station it is feasible to add further stations to the same computer. Each station consisting of an A.D.C., a C.R.O. display and a teletype console could be used independently as separate pulse height analysers or together in a multiparameter mode. It is predicted that up to five stations would be accommodated with only a small increase in dead time for individual stations.

9. REFERENCES

1. PDP-15 Systems Reference Manual. Digital Equipment Corp. Maynard, Mass. U.S.A.
2. PDP-15 Systems Interface Manual. Digital Equipment Corp. Maynard, Mass. U.S.A.
3. Series 2200 Analog to Digital Converter Instruction Manual, February 1968. Nuclear Data Inc. Illinois, U.S.A.
4. Model BWD 506 5 inch Single Beam Oscilloscope Manual. B.W.D. Electronics Pty. Ltd., Gardener, Vic. Australia.

APPENDIX 1

GLOSSARY OF CIRCUIT DIAGRAM ABBREVIATIONS

DCH GR	Data channel grant
ADC DCH FLAG	A.D.C. data channel flag
IO SYNC	Input-output synchronising pulses
DCH EN IN	Data channel enabled input
PWR CL	Power clear or reset
CLR RQ	Clear request for data channel
DCH RQ	Request data channel
ENA	Data channel enabled
INC MB	Increment memory buffer
DCH EN OUT	Data channel enabled output
ABORT	Abort A.D.C. transfer
DISPLAY FLAG	Display data channel flag
SIXTEENS	Delay pulse on every sixteenth dot
MARK OFLO	Mark mode overflow pulse
DISPLAY OFLO	Display mode overflow pulse
LOAD SW1	Load status word number 1
LOAD SW2	Load status word number 2
SHIFT Y-DATA	Shift-pulsed train

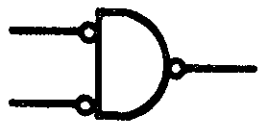
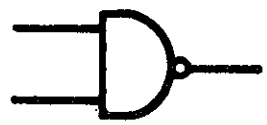
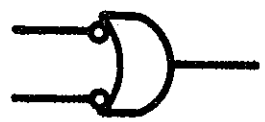
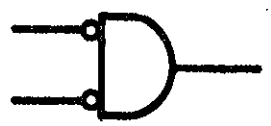
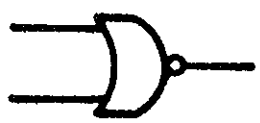
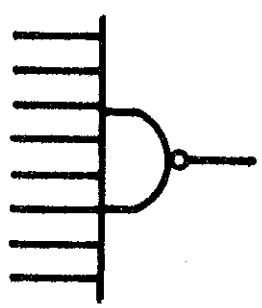
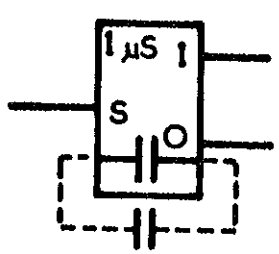
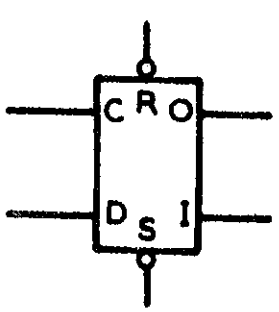
SYMBOL	FUNCTION	NAME	REMARKS
	OR-GATE	L623 OR L624	OPEN COLLECTOR OUTPUT 220 OHM DRIVER OR 50 OHM DRIVER
	NAND- GATE	L7400	
	NEGATIVE NOR-GATE		
	NEGATIVE NAND-GATE		
	NOR-GATE	L7402	
	8-INPUT NAND-GATE	L7430	
	ONE-SHOT	L803	ADDITIONAL DELAY WITH EXTERNAL CAPACITOR
	D-TYPE FLIP-FLOP	L7474	

FIGURE 1. TABLE OF SYMBOLS

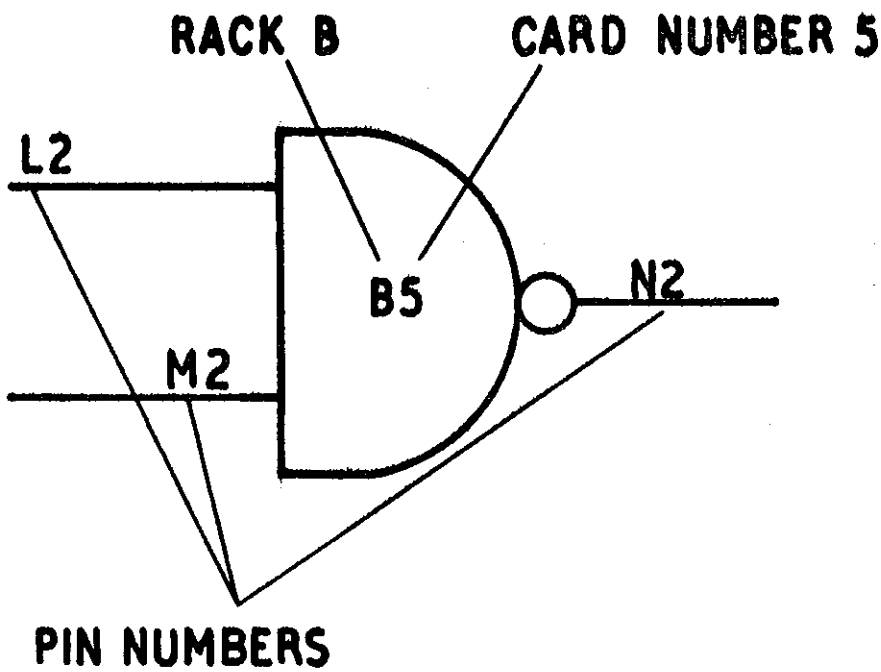


FIGURE 2. SYMBOL NOMENCLATURE

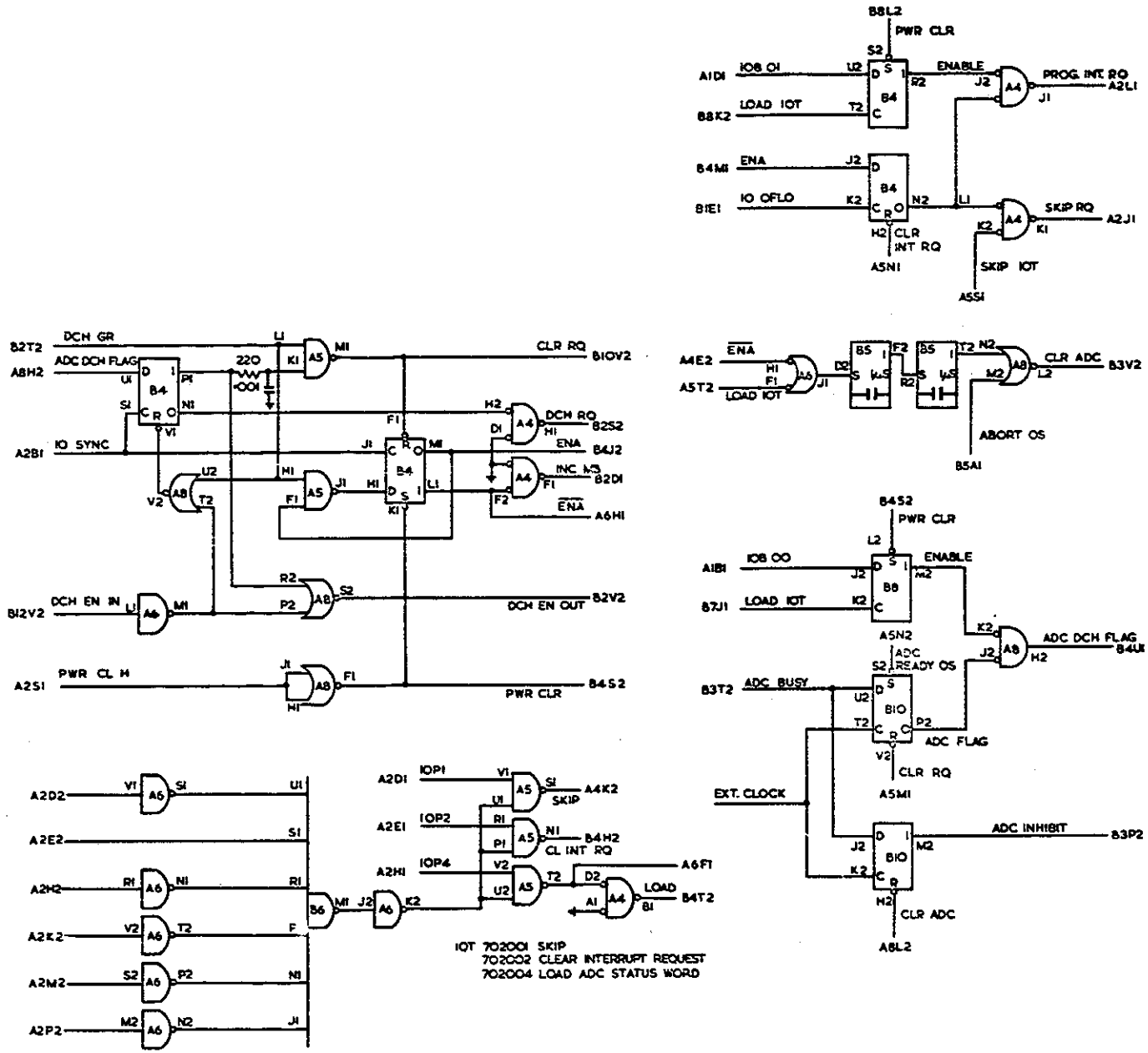


FIGURE 3. ADC INTERFACE DATA CHANNEL AND PROGRAMMED TRANSFER CONTROL

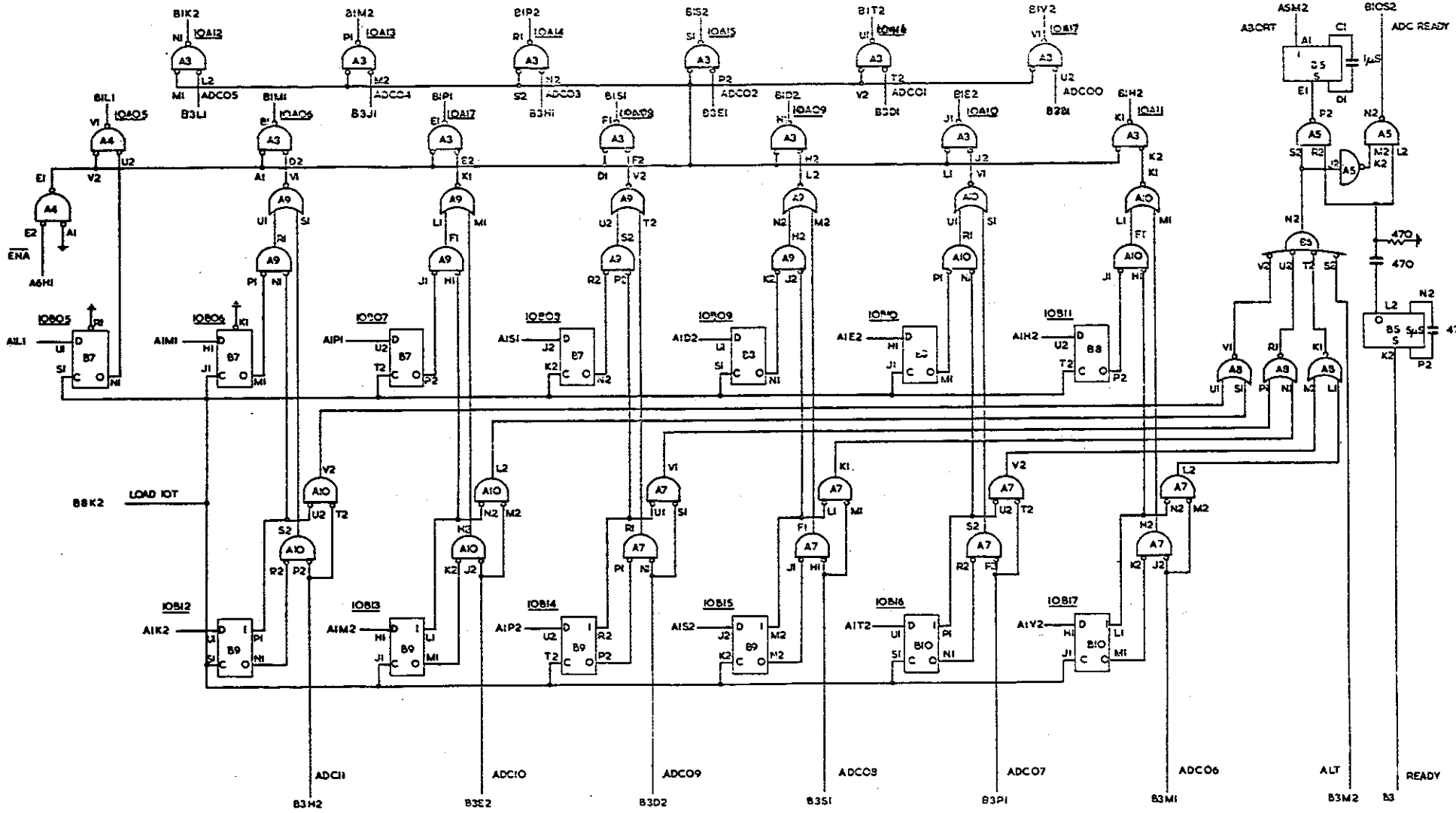


FIGURE 4. ADC INTERFACE RANGE AND STORAGE ADDRESS REGISTERS

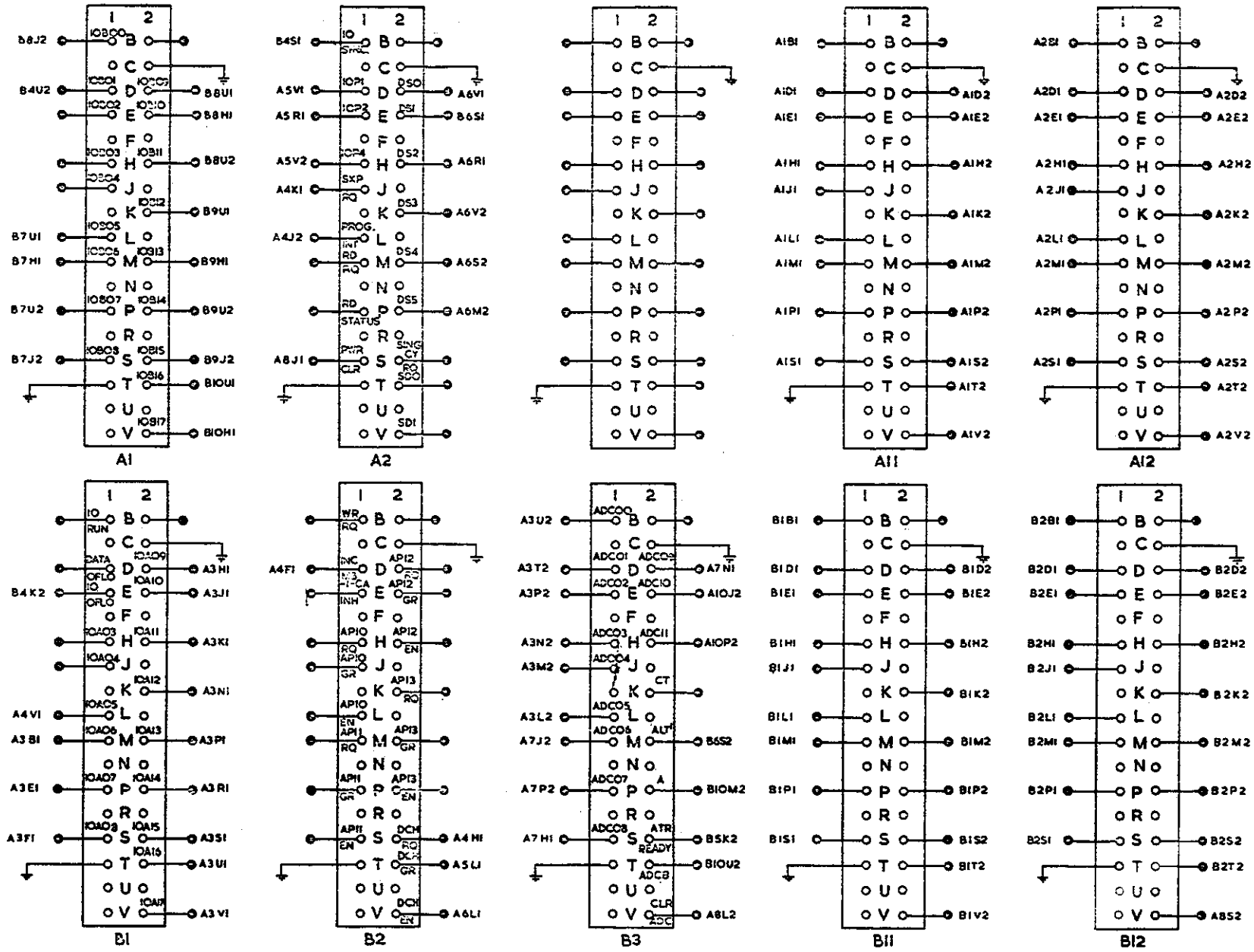


FIGURE 5. ADC INTERFACE INPUT-OUTPUT SCHEDULE

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
LO23	LO23	L624	L624	L7400	L7400	L7402	L7402	L7402	L7602	LO23	LO23																				
		3-12	2-5 3-2	2-5 3-3	2-8	3-8	2-5	3-8	3-8																						
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
LO23	LO23	LO23	L7474	L8O3	L7430	L2878	L7474	L7474	L7474	LO23	LO23																				
			2-4	2-2 3-2	2-1 3-1	3-4	2-1 3-3	3-4	2-2 3-2																						

SHEET NO. - NO. OF ELEMENTS

FIGURE 6. ADC INTERFACE CARD ALLOCATION SCHEDULE

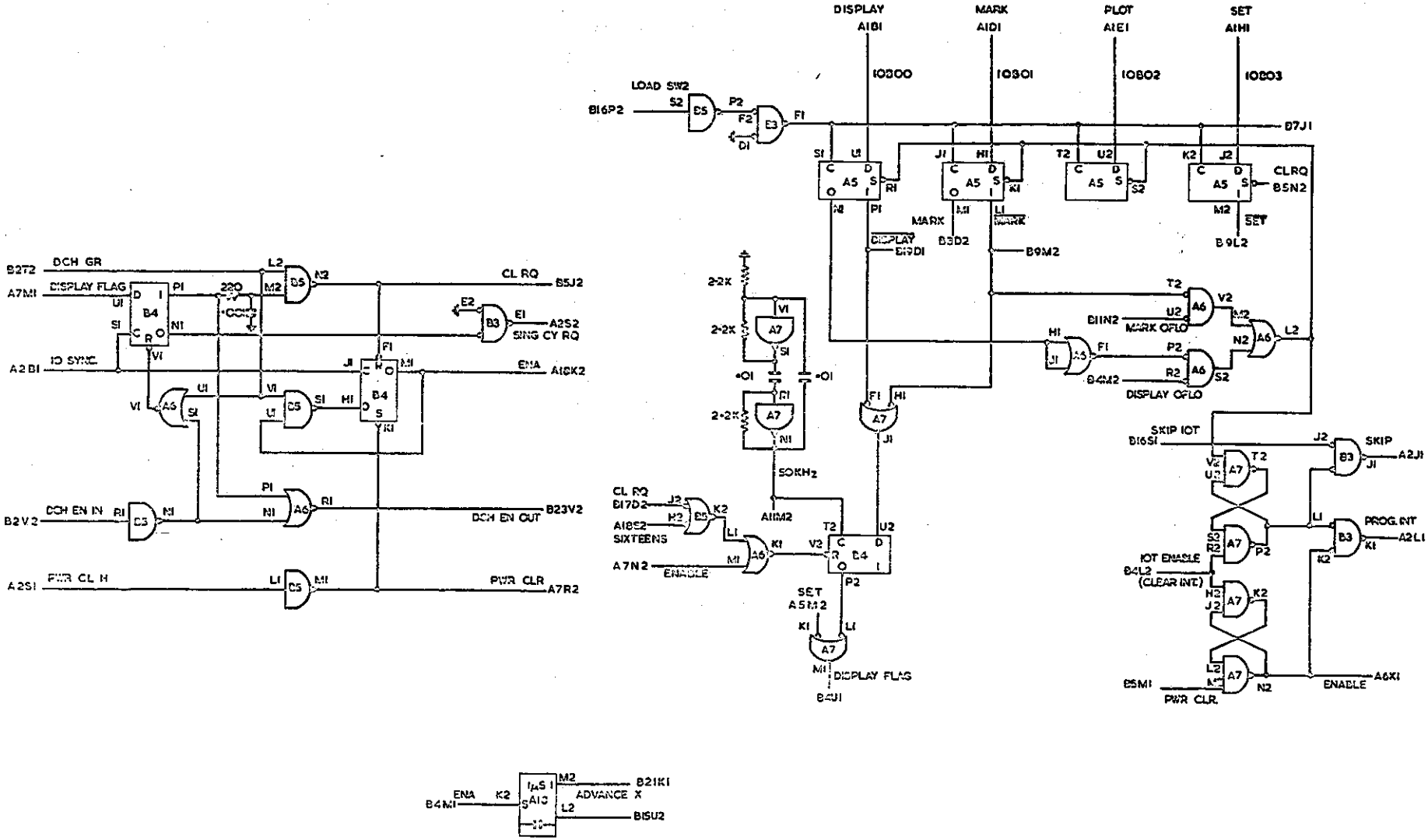
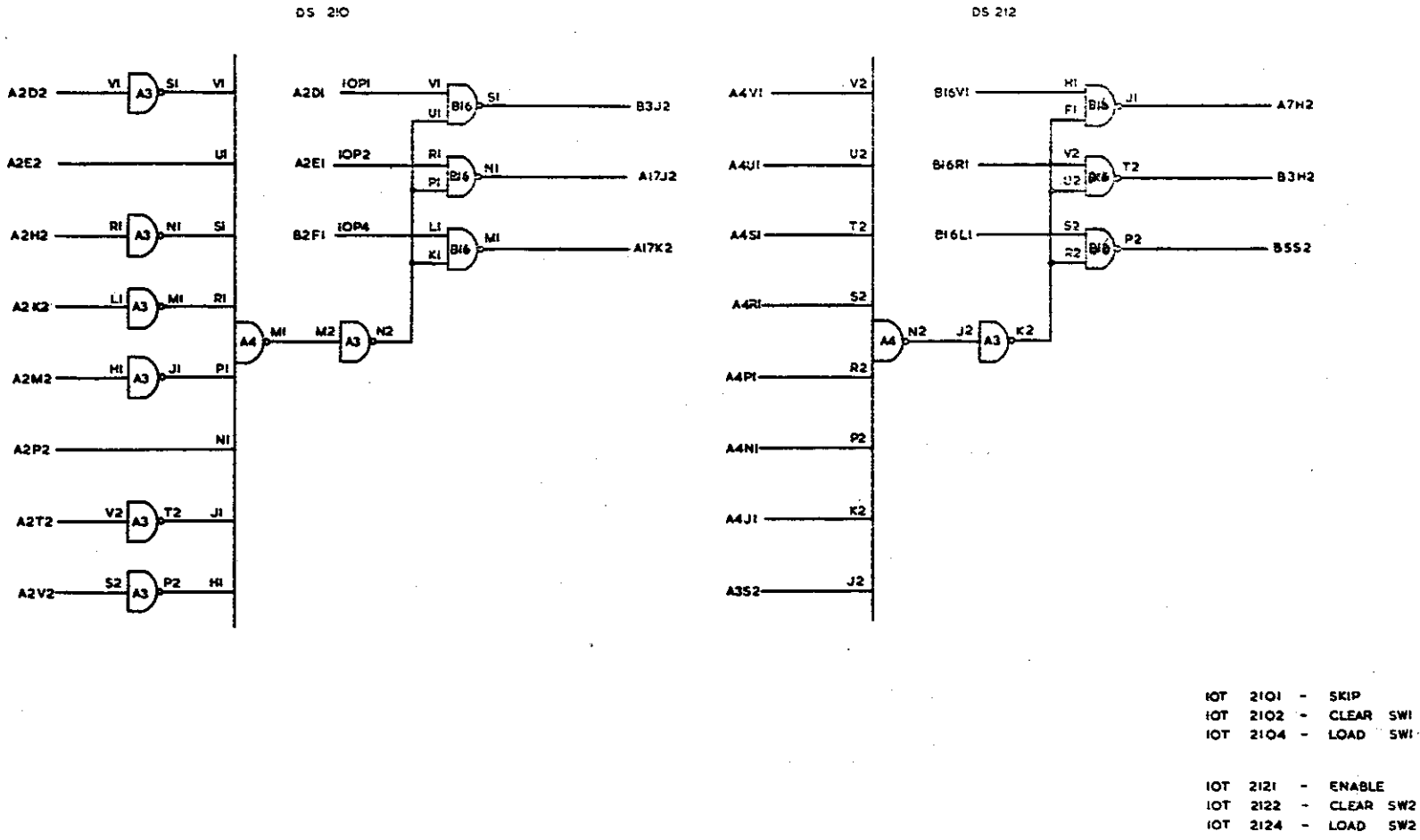


FIGURE 7. DISPLAY INTERFACE DATA CHANNEL I/O AND MODE REGISTER



IOT 2101 - SKIP
IOT 2102 - CLEAR SWI
IOT 2104 - LOAD SWI

IOT 2121 - ENABLE
IOT 2122 - CLEAR SW2
IOT 2124 - LOAD SW2

FIGURE 8. DISPLAY INTERFACE DEVICE SELECTORS

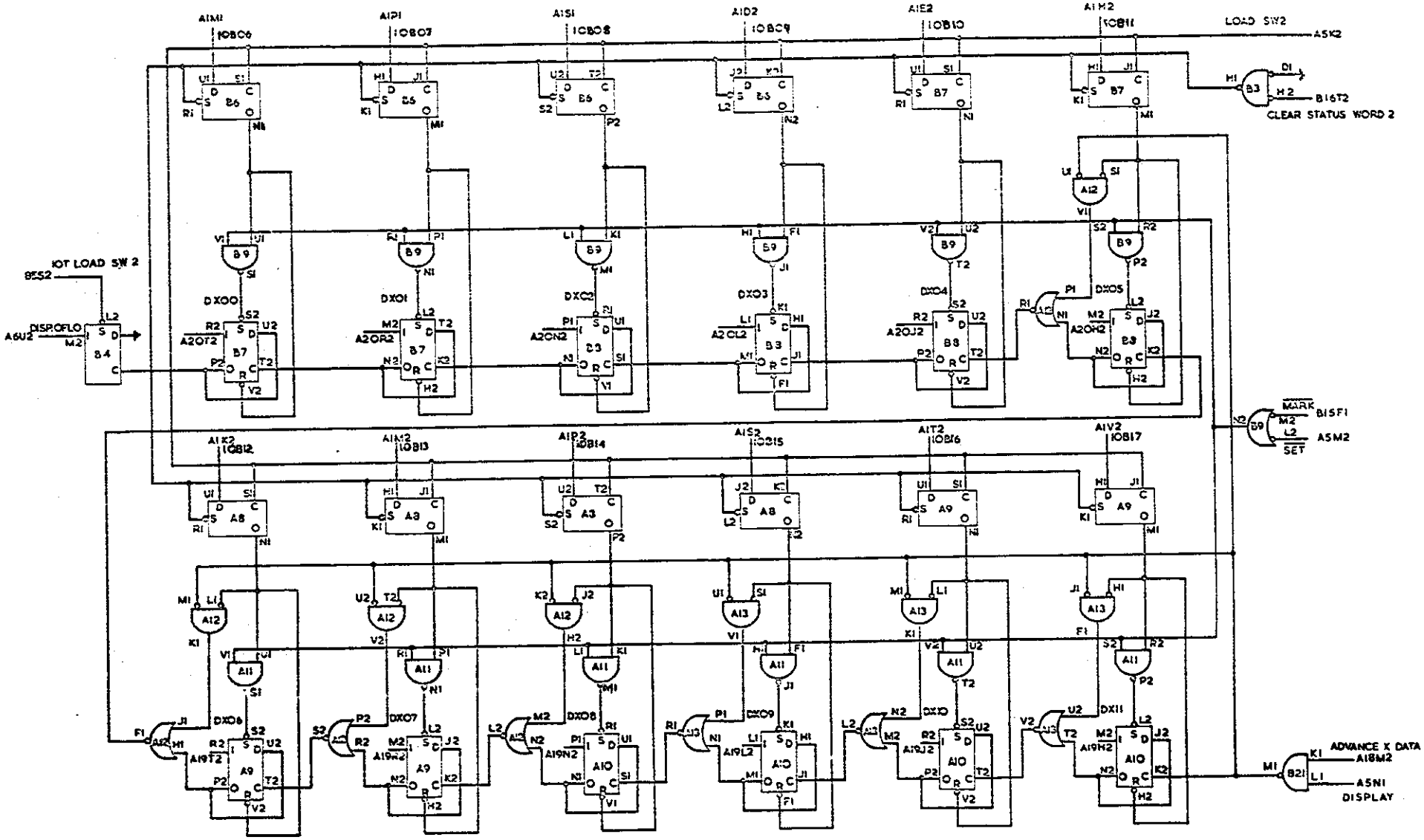


FIGURE 9. DISPLAY INTERFACE X-AXIS RANGE MARKERS

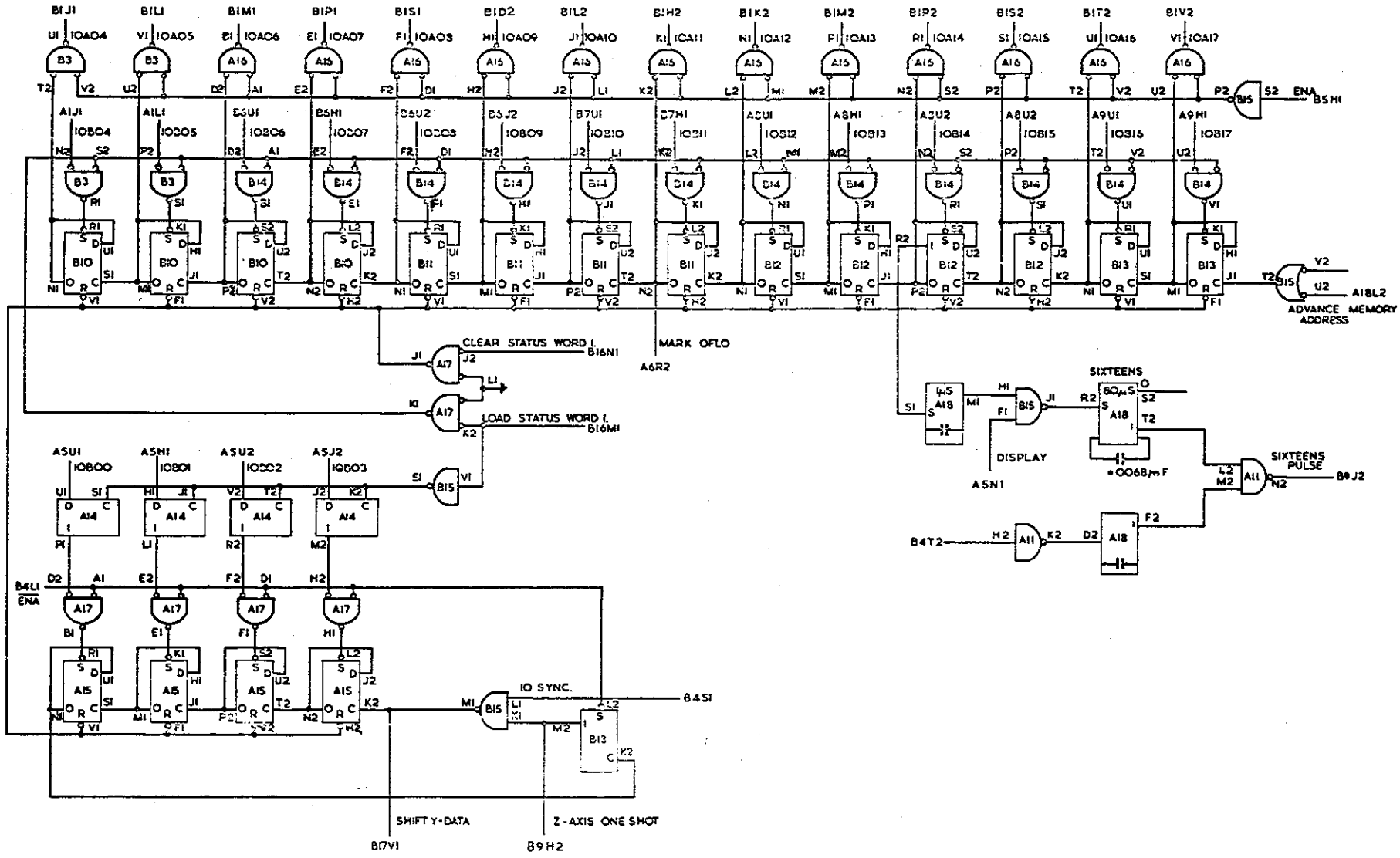


FIGURE 10. DISPLAY INTERFACE MEMORY ADDRESS REGISTER Y-AXIS SHIFT

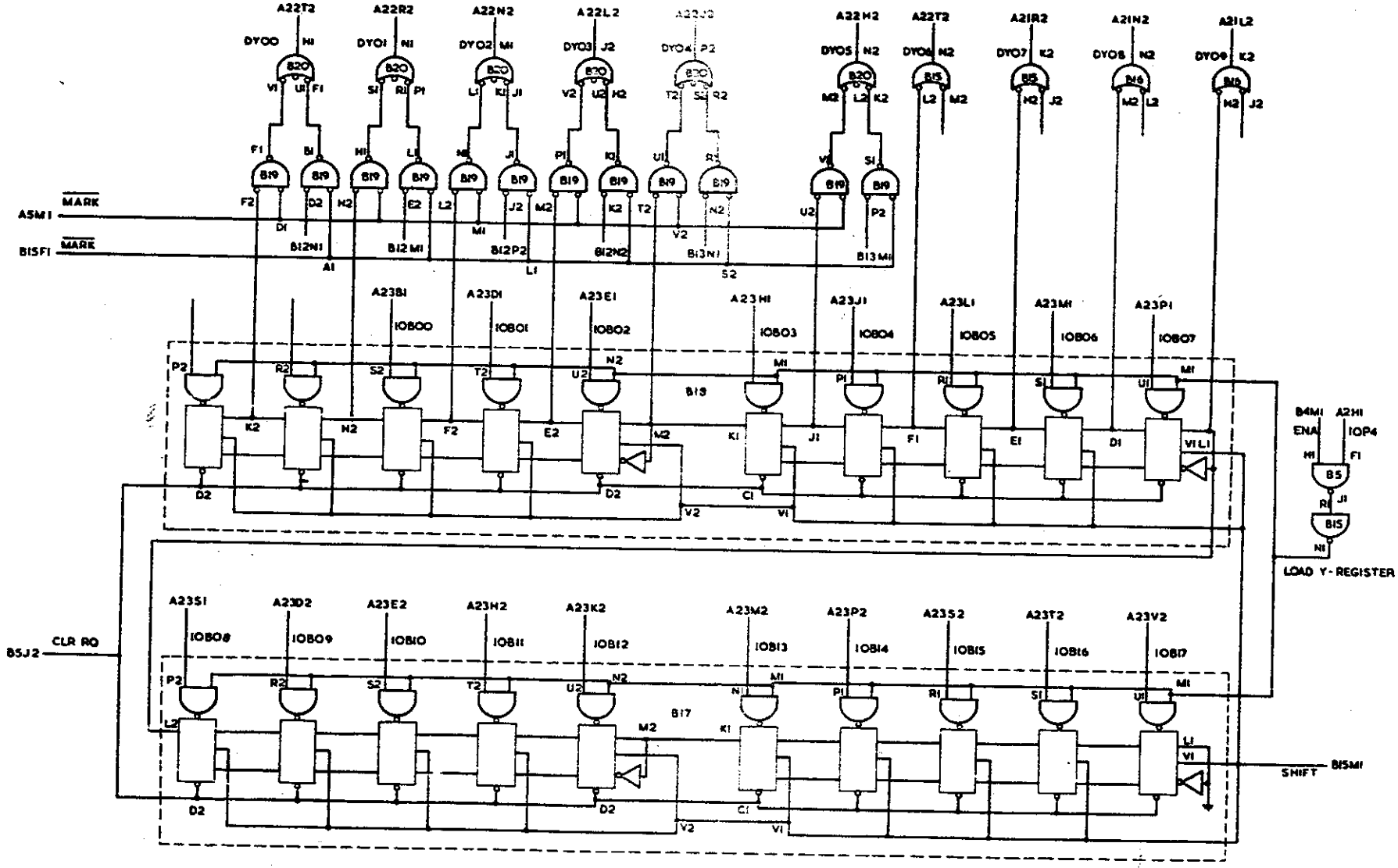


FIGURE 11. DISPLAY INTERFACE Y-AXIS DATA REGISTER

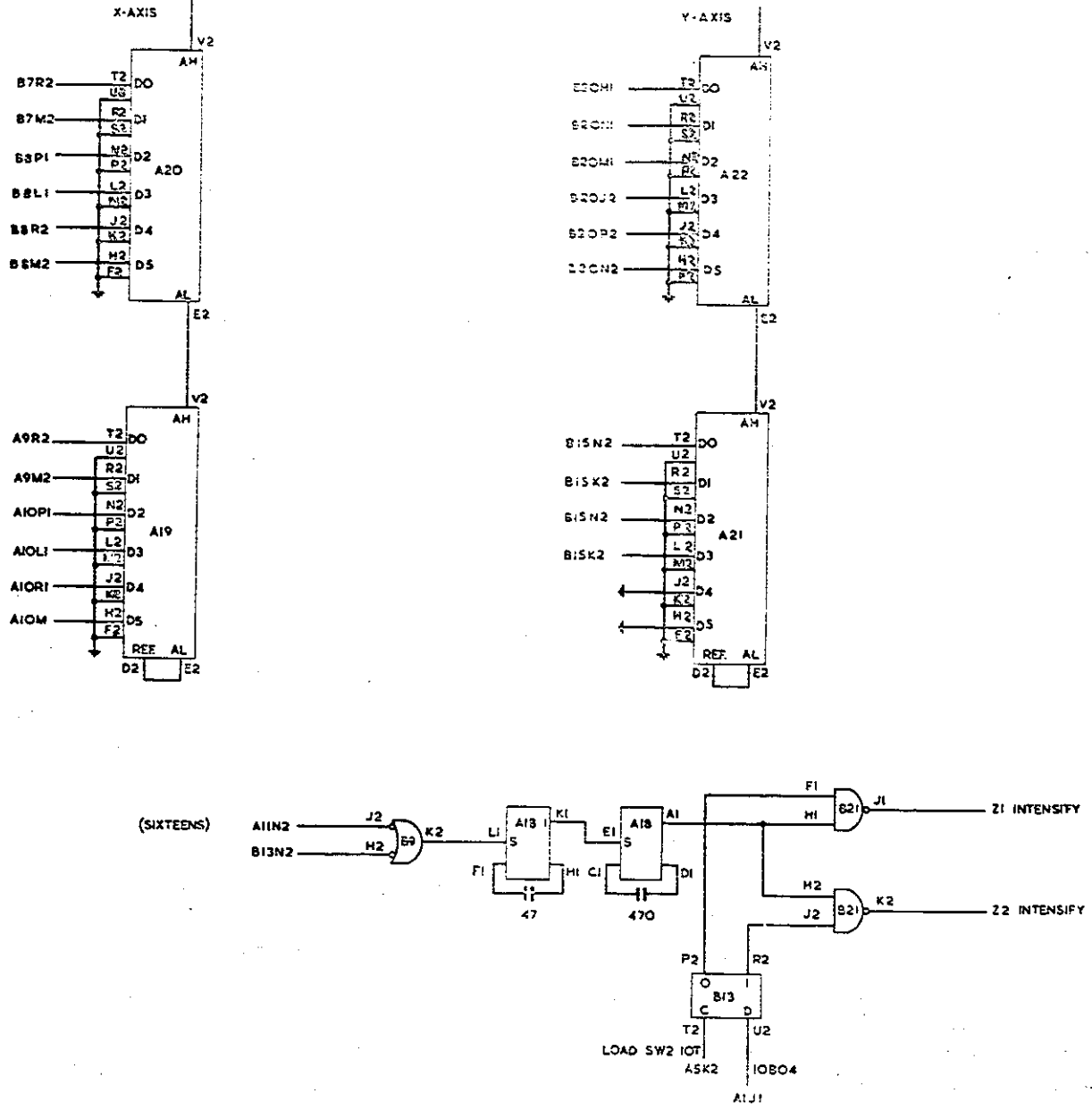


FIGURE 12. DISPLAY INTERFACE DIGITAL-TO-ANALOGUE CONVERTERS

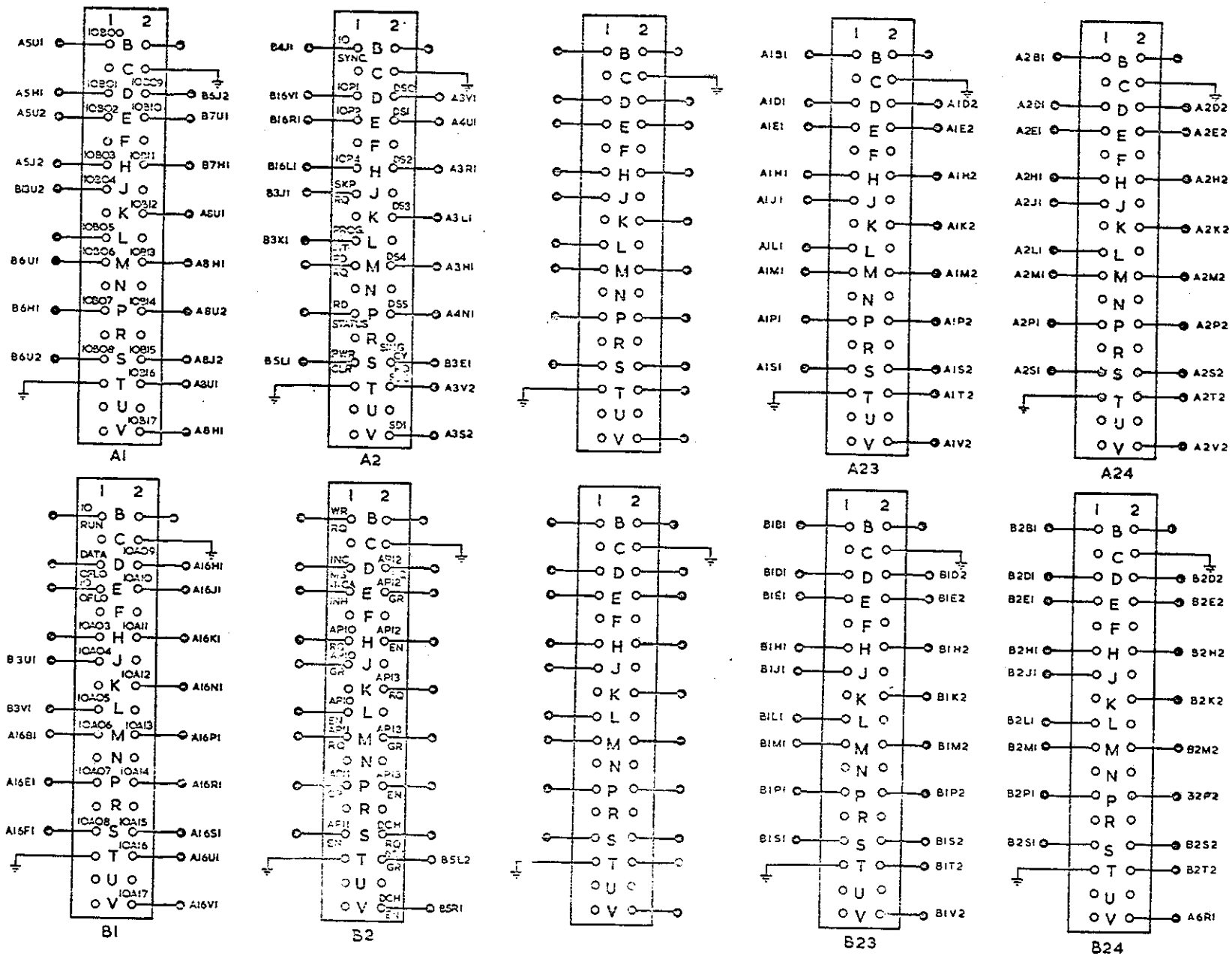


FIGURE 13. DISPLAY INTERFACE INPUT-OUTPUT SCHEDULE

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
L023	L023	L7400	L7430	L7474	L7402	L7400	L7474	L7474	L7474	L7400	L7403	L7400	L7474	L7474	L624	L623	L603	L600	L600	L600	L600	L023	L023								
		3-8	3-2	2-4	2-7	2-8	4-4	4-4	4-4	4-6 5-2	4-8	4-6	5-4	5-4	5-12	5-6	2-1 5-3 7-2	7-1	7-1	7-1	7-1										
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
L023	L023	L624	L7474	L7400	L7474	L7474	L7474	L7400	L7474	L7474	L7474	L7473	L623	L7400	L7400	L7406	L7496	L623	L7410	L7400		L023	L013								
		2-3 4-1 5-4	2-3 4-1	2-6 6-1	4-4	4-4	4-4	4-7 7-1	5-4	5-4	5-4	5-3 7-1	5-12	5-5 6-3	3-6 6-2	6-2	6-2	6-12	6-6	7-2 4-1											

SHEET NO - NO OF ELEMENTS

FIGURE 14. DISPLAY INTERFACE CARD ALLOCATION SCHEDULE